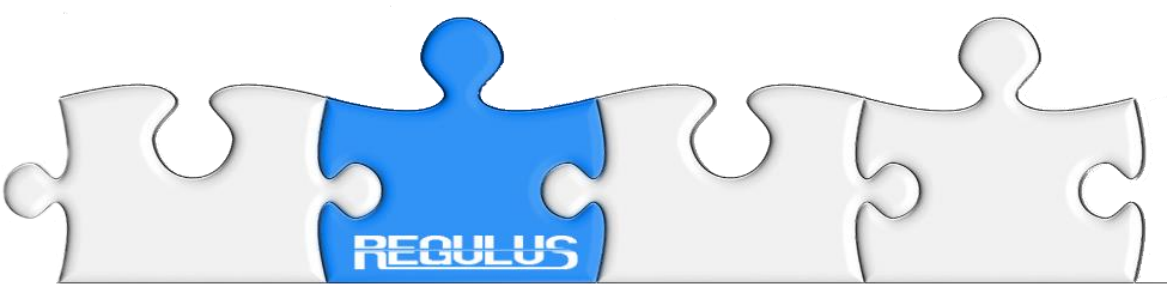
*u*REG

UNIVERSAL BAY CONTROLLER UNIT & PROTECTION RELAY

USER MANUAL

Version 1.14_ENG



SAFETY RULES

Operating or tested electric equipment is connected to sources supplying electric energy.
Therefore, some parts of the equipment may expose dangerous voltage. Also, for a certain period of time after disconnection, this voltage may continue to exist across some elements or equipment terminals. Failure to follow warnings or use the equipment properly may pose a hazard of injuries and/or cause damage to the equipment.

Proper and safe operation depends on proper transport and handling, appropriate storage, installation and final inspection prior to start-up, proper functioning as well as careful maintenance and service. Proper earthing of the equipment must be established.

Therefore, any work with the device and operation of the controller unit should be entrusted only to qualified personnel.

QUALIFIED PERSONNEL means any person who:

- is authorized to install, commission and operate equipment and the associated system,
- is authorized to perform switching operations in substation bays in accordance with safety instructions,
- is trained in safe equipment operation in accordance with standards,
- is trained in OH&S and first aid.

CAUTION

The documentation of the uREG relay contains necessary instructions relating to installation, start-up and operation of the equipment. However, it is not possible to mention all essential circumstances or detailed information regarding all probable concepts in this particular document. In case of any doubt or specific problem, please refrain from any action until an authorized confirmation is obtained. In this case, please consult technical staff at REGULUS to obtain necessary explanations.

DECLARATION OF CONFORMITY CE

Manufacturer:

REGULUS Zygmunt Liszyński,
ul. Bonin 20/28, 60-658 Poznań,
ul. Piątkowska 122/9 – 10, 60-649 Poznań,
Poland

hereby declares that

Universal Bay Controller and Protection Device: *u*REG®

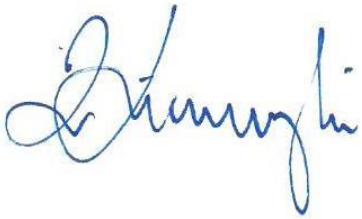
has been designed and manufactured in conformance with essential requirements provided in

Directive 2014/30/EU of the European Parliament and of the Council of 26 February 2014 on the harmonisation of the laws of the Member States relating to electromagnetic compatibility (recast)

and in accordance with recommendations provided in the following standards

PN-EN 60255-1:2010 (Measuring relays and protection equipment. Part 1: Common requirements),
PN-EN 60255-25:2002 (Electrical relays. Part 25: Electromagnetic emission tests for measuring relays and protection equipment),
PN-EN 60255-26:2013 (Measuring relays and protection equipment. Part 26: Electromagnetic compatibility requirements),
PN-EN 60255-27:2006 (Measuring relays and protection equipment. Part 27: Product safety requirements),
PN-EN 61000-6-2:2008 (Electromagnetic compatibility (EMC). Part 6-2 Generic standards. Immunity for industrial environments) and related standards.

The equipment shall be used in accordance with requirements provided in the operating manual.



2013.05.10. – 2018.07.16. Zygmunt Liszyński

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1. INTRODUCTION & INTENDED USE

***u*REG®** is a *u*niversal Intelligent Electronic Device (IED) providing fault protection, measurements, control, communication, logging, to be operated together with automation solutions installed in MV and HV power system substations.

*u*REG is based on many years of experience gained by its designers during development, production and operation of previous versions: *u*CZIP and systems such as CZIP and CZIP-1,2,3,4.

Applications of *u*REG include:

- commercial power industry,
- power stations and CHP plants,
- wind and hydroelectric power stations, biogas plants, cogeneration, photovoltaics, etc.,
- industry.

*u*REG provides protective functions for equipment and consumer devices associated with a bay in the scope of different fault criteria: over and undercurrent, over and undervoltage, admittance, over and underfrequency, power, delay and non-delay, measurements and logging of electrical quantities as well as execution of substation automatic controls.

A modular flexible hardware design of the equipment ensures maximum adaptation to the scheme of a specific application in the power sector and industry. Also, it guarantees optimization of project expenditures by providing high functionality, even if the simplest configuration is selected.

Three versions of operator panels (including two panels with high resolution color displays), with a wide range of I/O modules and options of enclosure installation methods can be used to customize the equipment to individual needs.

The device supports many transmission protocols (including DNP3 and IEC-60870) to ensure communication conforming to currently applicable and, by compliance with IEC-61850, also upcoming standards. Also, *u*REG is designed for operation together with a supervisory system or locally via PTP IEEE1588 for precise time synchronization of devices.

Hardware unification enables dedicating *u*REG to a specific bay, mostly by means of its software (**APPLICATION**), with the hardware-based approach limited to a minimum.

2. SCOPE OF THE MANUAL

This manual relates to *u*REG which is a common hardware/software base for comprehensive bay operations in a power system substation with regards to protective functions, measurements, controls, communication, logging and operation together with substation automation solutions.

The part of *u*REG defining soft functionality (ie. dedication to a specific bay) is referred to as **APPLICATION** (Applications are described in a separate manual).

3. FUNCTIONS AND FEATURES (depending on the developed APPLICATION)

The most important features:

- **Short-circuit overcurrent fault protection (ANSI 50/51)** from effects of line-to-line short-circuit fault with an independent single-stage characteristic curve. For the short time after operational power-up of a bay, current and time settings can be dynamically modified by adjustable increments to shift the tripping shutdown point. Increments become inactive after successful closing. The protection function can be deactivated. Activation is possible.
- **Time-dependent overcurrent protection (51)** provides three dependent time-current characteristic curves with a different slope: moderate, standard and rapid. Tripped protection results in shutdown. The protection function can be shut down.
- **Overcurrent protection against overloading (51)** with one-stage feature. The protection can be shut down, set to respond to a signal or trip-out.
- **Negative sequence overcurrent fault protection (51_2).**
- **Directional power interlock (32) for any protective function (67).**
- **Voltage (59) protective functions** including the **overvoltage (59P) fault protection** and the **undervoltage (59U) fault protection**, both of which have independent characteristic curves; they are of single-stage type; optionally to be shut down; they can cause local and general-substation (UP) alarms or tripping; for both cases, it is possible to select the increase (decrease) mode for one voltage or all voltages simultaneously.
- **Line-to-earth short-circuit fault protections group** according to selectable criteria relating to: overcurrent (directional or nondirectional)with an independent characteristic curve, admittance and susceptance. The unit is equipped with a common input for Ferranti-Holmgreen filters. Protective functions can be shut down, and used to activate local or substation (UP) alarms or cause trip-out. Admittance criteria are activated once threshold U0> (predefined by setting) is exceeded.
- **Under (81L) and overfrequency (81O) fault protection.**
- **Derived frequency criterion (df/dt) (81R – Rate-Of-Change Of Frequency).**
- **'Vector shift' criterion** (three-phase type), adjustable within the range of 1 to 25 angle degrees (measuring accuracy 0.5 deg), instantaneous (internal time approx. 30 ms).
- **Current asymmetry criterion (60P).**
- **Differential fault protection (87, 87T, 87G)** for each phase with multi-slope bias characteristics and selectable slope knee point. Ideally suited for the protection of transformers with two or three windings configured in one of the most popular vector group (Yy0,Yy6,Yd1,Yd5,Yd7,Yd11). In this case 2^{nd} and 5^{th} harmonic restraint functions can be applied. The differential protection function is also suitable for generators and large motors against two or three phase internal faults and inter-turn faults.
- **Three-phase overpower (P3f>) and underpower (P3f<) protection for active power** with an 1-second average, adjustable for the active power value across device terminals within the range of 10 to 1000 W (easily converted into primary power by multiplying the setting by the thetaIf current transformation ratio and voltage transformation ration – i.e. 150 for the 15 kV grid), with directional setting in three modes: non-directional, positive power direction, negative power direction.
- **Three-phase overpower (Q3f>) and underpower (Q3f<) protection for reactive power** with an 1-minute average, adjustable for the reactive power value across device terminals within the range of 10 to -1000 var (easily converted into primary power by multiplying the setting by the thetaIf current transformation ratio and voltage transformation ration – i.e. 150 for the 15 kV grid), with directional setting in three modes: non-directional, positive power direction, negative power direction.
- **Cooperation with external protective devices** via terminals of input signals.

- **Distributed busbar protection** in incoming feeders and **busbar protection interlock** in outgoing feeders (activated if current setting IZS>> is exceeded).
- **Closing interlocks for any selectable criteria.**
- **Distributed multistage smart load (SCO) and load restoration (Reclose the circuit breaker after tripping ANSI 79 - SPZ/SCO) automation** and/or **two-stage SCO automation, centralized with SPZ/SCO.**
- **Capability to operate together with other substation automation solutions** – start-up of a local circuit-breaker failure protection (LRW) with a separated contact-type input.

- **Operation together with** current transformers with the rated secondary current of 1 A or 5 A.
- **Support of the following configurations of busbars disconnectors:**
  a) single-type busbars:
  - disconnectors in conventional configurations,
  - three-position disconnectors, including disconnector-earthing switch,
  - switchgear w/ withdrawable circuit-breaker segment,
  b) double-type busbars:
  - two systems of disconnectors,
  - disconnector-earthing switch and disconnector.

- **Control of circuit-breaker and electric driving mechanism of bay disconnectors** (depending on the current **APPLICATION** version, the control is operated via keyboard using three additional buttons; operation together with a conventional controller is optional).
- **Summation of braking currents** (switched Amperes) by the circuit-breaker in four adjustable ranges.
- **Interlock** against "surging", i.e. multiple closing operations of the circuit-breaker during short-circuit.
- **Switch-off and switch-on heavy contacts relays** (type SR6 – number of relays depending on module configuration), **dedicated to operate together with circuit-breaker coils** (in emergency, the contact can break a circuit with a typical breaker coil resistance of 185 Ohm without risk of damage. The number of such emergency operations is up to 300.
- **Make-contact SPST NO and change-over relays SPDT** (number depending on module configuration), used to fulfill additional functions.
- **Free allocation of digital inputs** (physical terminals and computer inputs) and **relay outputs** to selected functions of the application.
- Unipolar and bipolar **digital inputs** (number depending on module configuration), including inputs with a programmable sensitivity threshold setting >20/>50 V DC and bipolar inputs (with 220/24 V DC input resistance to be readjusted by program).
  All logic inputs and outputs are programmable, independently of whether they are described in external wiring diagrams as dedicated to a specific function or not.

- **Visual signaling** on the LCD screen (**QVGA color** or alphanumeric – 2x16 characters), programmable LEDs (monochromatic or two-color) – depending on the operator panel type, two diodes to indicate the circuit-breaker status (for configurations w/o graphic display), diode to indicate proper device operation, diode AW to indicate emergency shutdown, diode UP to indicate bay supervision request and diodes to indicate activity of interfaces, and remote control interlock (BTS) diodes.

- **Conventional remote control (telemechanics)** by wired circuits for receiving/transmitting signals (via terminal inputs/outputs) as an alternative to communication channels.
- **Operation of substations switchgear** with SF6 and enclosed switchgears (support of relief vents).
- **Measurements** of true RMS values for 12 analog voltage and current signals, power coefficient tgφ or cosφ and derivative values: frequency, active/reactive power and selected type of energy (including subdivision into day-time zones) and admittance, conductance and susceptance of earth fault branch (conditionally, when U0>U0n is satisfied), based on calculated RMS values.

- Up to **4 banks for main settings + 1 bank for auxiliary settings** (for transmission channels set-points purposes).
- **Event log recorder** which can save **1024 reports (stored in non-volatile memory)**, each day and time-stamped with resolution up to 100us, event code as protocol index (e.g. DNP3), and user definable description.
- **Data recorder (DAR)** which records recent samples in an active circular buffer; in a standard version, buffer memory can be organized in one of the following buffer configurations: 2 * 20.48s (ie. 2 buffers, each of 20.48s) , 4 * 10.24s, 8 * 5.12s, 16 * 2.56s, 32 * 1.28s, 2 * 40.96s, 4 * 20.48s, 8 * 10.24s, 16 * 5.12s or 32 * 2.56s.
  There are always **10 electrical quantities** recorded in each buffer.
  → Example: configuration with CT-0 + VT-0:
  • Voltage U12 • Current I1
  • Voltage U23 • Current I2
  • Voltage U31 • Current I3
  • Voltage U0 • Current I0
  • Input AUXI0 (VT) • Current Ig
  and **96 digital values** (states of functors).
  For IF-4 modules, the range of buffer configuration is extended by the following settings:
  2 * 81.92 s, 4 * 40.96 s, 8 * 20.48 s, 16 * 10.24 s and 32 * 5.12 s.
  In addition, the IF-4 module (combined with MB-2/3) provides a data recorder operating at 3200 Hz (64 samples per period) and even a wider buffer configuration range and up to **192 digital states** to be recorded.
- **Criteria recorder (CDAR)** – records up to 16 selectable RMS values in max. 32 buffers with settable recording frequency.
- **Time synchronization acc. to IEEE 1588 PTP with a precision of 1 us** with autonomic local synchronization (if no supervisory system is present).
- **Operation together with a supervisory system via:**
  – two independent **RS-485** links – to be selected with one of many transmission protocols: uCZIPstd, uCZIPnet, DNP-3.0, IEC-60870-5-101, IEC-60870-5-103, CZIPstd (backward compatibility), Modbus, CAN-PPM2, etc. It is possible to use optical fiber cables (FO);
  – 10/100 Mb **Ethernet** link – to be selected with TCP / UDP protocols (with protocol tunneling: uCZIPstd, DNP-3.0, etc.) and IEC-60870-5-104.
- **Operation with a local PC** via independent communication interfaces: **RS232** and **USB** (via uCZIPstd and uCZIPnet).

- **Self-check** of operational correctness of important unit elements; all semiconductor components are manufactured according to reliable static logic (also in case of memory) for industrial applications.
- **Software upgrade** – all software components (both firmware and the **APPLICATION** for a given bay) can be reprogrammed via RS-232, RS-485 and USB.

- **Access to change settings** via operator panel keyboard, secured by a two-level user code (two buttons pressed in a defined sequence). Changing settings via PC requires no password. The manufacturer recommends changing settings via PC since this approach is simple.
- **Universal power supply** by DC or AC within a wide voltage range, optionally “hot standby” (two power units); quick operational readiness after device powering-up (typically 3.5 seconds).

4. TECHNICAL DATA

Phase current input circuits

Rated current In	5 A or 1A
Measurement range	0 ÷ 192 A
Measurement error within ranges:	0.05 ÷ 0.35 A <5 %
	0.35 ÷ 50 A <1.5 %
	50 ÷ 192 A <5 %
Power input at I=In	<0.5 VA
Rated frequency fn	50 Hz
Continuous current-carrying capacity	3 * In
1-second thermal endurance	100 * In
Dynamic withstand value (surge current)	250 * In

Phase voltage input circuits [VT-0, VT-2, VT-3]

Rated voltage Un	100 V
Measurement range	0 ÷ 130 V
Measurement error within the measuring range	<1.5 %
Power input at U=Un	<0.4 VA
Rated frequency fn	50 Hz
Continuous voltage endurance*	1.4 * Un

Phase voltage input circuits [VT-1, VT-4, VT-5, VT-7, VT-8]

Rated voltage Un	230 V
Measurement range	5 ÷ 500 V
Measurement error within the measuring range	<3 %
Power input at U=Un	<1 VA
Rated frequency fn	50 Hz
Continuous voltage endurance*	1.5 * Un

Zero-sequence current input circuit

Rated current Ion	1 A
Measurement range	0 ÷ 10 A
Measurement error within ranges:	3 ÷ 25 mA <5 %
	25 mA ÷ 3.5 A<1.5 %
	3.5 ÷ 10 A <5 %
Power input at I=Ion	<0.28 VA
Rated frequency fn	50 Hz
Continuous current-carrying capacity	3 * Ion
1-second thermal endurance	100 * In
Dynamic withstand value (surge current)	250 * Ion

Forceful short-circuit overcurrent protection

Tripping current setting range I>>	0.9 ÷ 100 A or 0.1 ÷ 50 A
Internal operate time for 2-fold overcurrent value	20 ÷ 50 ms (typical 35 ms)
Adjustable resetting ratio	0.910 ÷ 0.985

Dependent overcurrent protection

Activity and mode of the dependent criterion RI >	inactive, OW
Overcurrent-stage starting current I>	0.3...50 A
Time delay of 2-fold overcurrent tI>	0.05...24 s
Slope of the dependent characteristic curve wtI >	moderate, standard, rapid

Short-circuit overcurrent protection

Tripping current setting range I>	0.1 ÷ 50 A
Internal operate time time for 2-fold overcurrent value	20 ÷ 50 ms (typical 35 ms)
Adjustable resetting ratio	0.910 ÷ 0.985

Differential overcurrent protection

Internal operate time for 2-fold overcurrent value	15 ÷ 40 ms (typical 22 ms)
Internal operate time with harmonic lock-out	25 ÷ 50 ms (typical 30 ms)
Inrush stabilization (harmonic restraint deviation)	+- 10%

Overvoltage protection [VT-0, VT-2, VT-3]

Line-to-line operating voltage of overvoltage protection U>	5 ÷ 130 V
Internal operate time for 2-fold value of exceeded setting	20 ÷ 50 ms (typical 35 ms)
Adjustable resetting ratio	0.910 ÷ 0.985

Undervoltage protection [VT-0, VT-2, VT-3]

Line-to-line operating voltage of undervoltage protection U<	5 ÷ 130 V
Internal operate time for 2-fold value of exceeded setting	20 ÷ 50 ms (typical 35 ms)
Adjustable resetting ratio	1.015 ÷ 1.059

Under and overfrequency protection

Minimum voltage threshold of protection start-up f< and f>	18 V
Internal operate time for 2-fold value of exceeded setting	60 ÷ 85 ms (typical 65 ms)
Adjustable resetting ratio for f> and f<	0.05 Hz
Measurement range	45 – 55 Hz
Frequency measurement deviation	+- 3 mHz max.

df/dt frequency derivative protection (ROCOF)

Minimum voltage threshold of protection start-up df/dt	18 V
Internal operate time for 2-fold value exceeded threshold	60 ÷ 85 ms (typical 65 ms)
Adjustable resetting ratio for f<	0.910 ÷ 0.985
Measurement range	0.1 – 25 Hz/s

Protection against contact lost with power grid (*Vector Shift*)

Recognized vector shift of line-to-line voltage vectors (in 3-phase)
within the range 0 to 60° with an accuracy of 0.5°; adjustable within 1 - 25°

Internal operate time	app. 30 ms

Line-to-earth short-circuit fault protection

Starting current of Io>	50 ÷ 5000 mA
Internal start-up time for 2-fold value of exceeded setting	20 ÷ 50 ms (typical 35 ms)
Adjustable resetting ratio	0.910 ÷ 0.985
Admittance non directional protective functions	Y0>, G0>
Admittance directional protective functions	G0k>, B0k>
Current I0 vs. voltage U0 phase angle correction: fii	-90° ÷ +90°
Starting admittance Y0>	0.50 ÷ 50 mS
Internal start-up time for 2-fold value of exceeded setting	50 ÷ 75 ms (typical 60 ms)
Adjustable resetting ratio	0.910 ÷ 0.985
Starting conductance G0>, G0k>	0.50 ÷ 5.0 mS
Internal start-up time for 2-fold value of exceeded setting	50 ÷ 75 ms (typical 60 ms)
Adjustable resetting ratio	0.910 ÷ 0.985
Starting susceptance B0k>	0.50 ÷ 5.0 mS
Internal start-up time for 2-fold value of exceeded setting	50 ÷ 75 ms (typical 60 ms)
Adjustable resetting ratio	0.910 ÷ 0.985

Busbar protection interlock

Starting current of busbar protection interlock IZS>>	0.1 ÷ 50 A or 0.9 ÷ 100 A
Internal start-up time for 2-fold value of exceeded setting	20 ÷ 50 ms (typical 35 ms)
Adjustable resetting ratio	0.910 ÷ 0.985

Binary input circuits (IO-0 module):

Remote control (telemechanics) circuits	
- rated input voltage (adjustable by settings)	24 V or 220 V DC
- input voltage range (24V)	17 ÷ 32 V
or (220 V)	88 ÷ 253V
- current input at 24 V or 220 V	<3 mA
Other circuits:	
- input voltage	88 ÷ 253 V
- current input at 220 V	< 3 mA
Special ordering option: AC inputs	230 VAC

Remote control (telemechanics) circuits (CM and CR modules):

- rated input voltage (adjustable by settings)	>20 V or >50 V
- input voltage range (24V)	20 ÷ 36 V
or (220 V)	50 ÷ 253 V
- current input at 24 V or 220 V	<3 mA
Other circuits:	
- input voltage	88 ÷ 253 V
- current input at 220 V	< 3 mA
Special ordering option: AC inputs	230 VAC

Signaling relay output circuits

Rated voltage		220 V DC
Continuous current-carrying capacity		1 A
Inductive circuit breaking:	220 V DC, L/R= 40 ms	0.1 A
or		
Rated voltage		250 V AC
Continuous current-carrying capacity		5 A
Breaking capacity:	220 V AC, cos ϕ=0.4	2 A

High-break contacts relay for use with the circuit-breaker coils

OW and ZW outputs:		
Rated voltage		220 V DC
Continuous current-carrying capacity		2 A
Inductive circuit breaking:	220 V DC, L/R= 40 ms	1.2 A / 300 cycles
or		
Rated voltage		250 V AC
Breaking capacity		8 A

Absolute accuracy of time delays

Delays acc. to precise setting	±1.5 ms
Delays acc. to accurate setting	±20 ms
Delays acc. to rough setting	±1 s
Delays acc. to long-time setting	±1 s

Input signals absolute positioning accuracy

For DC logic input signals	<16 ms
For AC logic input signals	25 ÷ 40 ms

Explanation: This value results from filtration or input signal computation.

Power supply (PS-0)

Rated supply voltage		220 VDC (or 230 VAC)
Admissible range of supply voltage changes	DC	88 ÷ 365 V DC
Admissible range of supply voltage changes	AC	100 ÷ 260 V AC
Power input at 220 V DC		<15 W (typ. 7.5W)
Device readiness after power-up		3.5 s

Power supply (PS-1)

Rated supply voltage		24 VDC
Admissible range of supply voltage changes	DC	21 ÷ 38 V DC
Power input at 24 V DC		<15 W (typ. 7.5W)
Device readiness after power-up		3.5 s

Insulation electric strength

For input circuits:	- sinusoidal voltage	2 kV/60 s/0.5 kVA
	- surge impulse voltage	5 kV/ 1.2/50 μs/0.5 J
Contacts of relays	- sinusoidal voltage	1 kV/60 s/0.5 kVA
I/O power unit	- sinusoidal voltage	2.5 kV/60 s/0.5 kVA

Immunity to external interference

Interfering signal	2.5 kV/1 MHz/400 ud/s

Environmental conditions

Ambient temperature	-5 °C...+55 °C
Storage temperature	-25 °C...+70 °C
Atmospheric pressure	>800 hPa
Relative humidity	<75% - no condensation or frost and ice formation inside case

Housing

High-grade steel (A4), acid-proof	
Panel flush mounting and panel surface mounting:	vertical / horizontal / lateral
IP rating of flush-mount enclosure:	
- on the panel side	IP 52
- on the terminal side	IP 40
IP rating of panel surface-mount enclosure:	IP 53

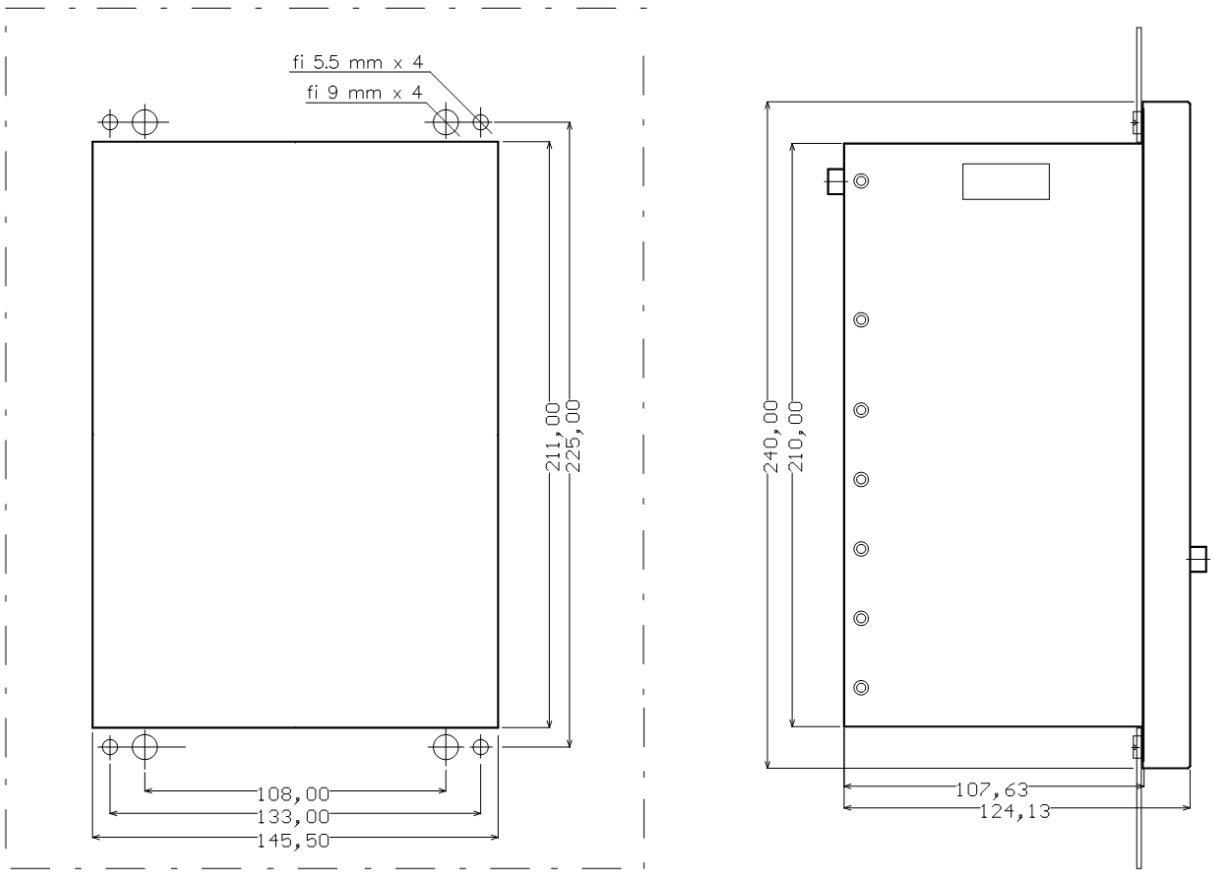
External dimensions and weight (7-slot enclosure)

Dimensions (integrated panel)	H x W x D
- flush mounting:	240 x 150 x 124 mm
- panel surface mounting:	270 x 150 x 200 mm
Weight	3.5 kg

Serviceable elements none

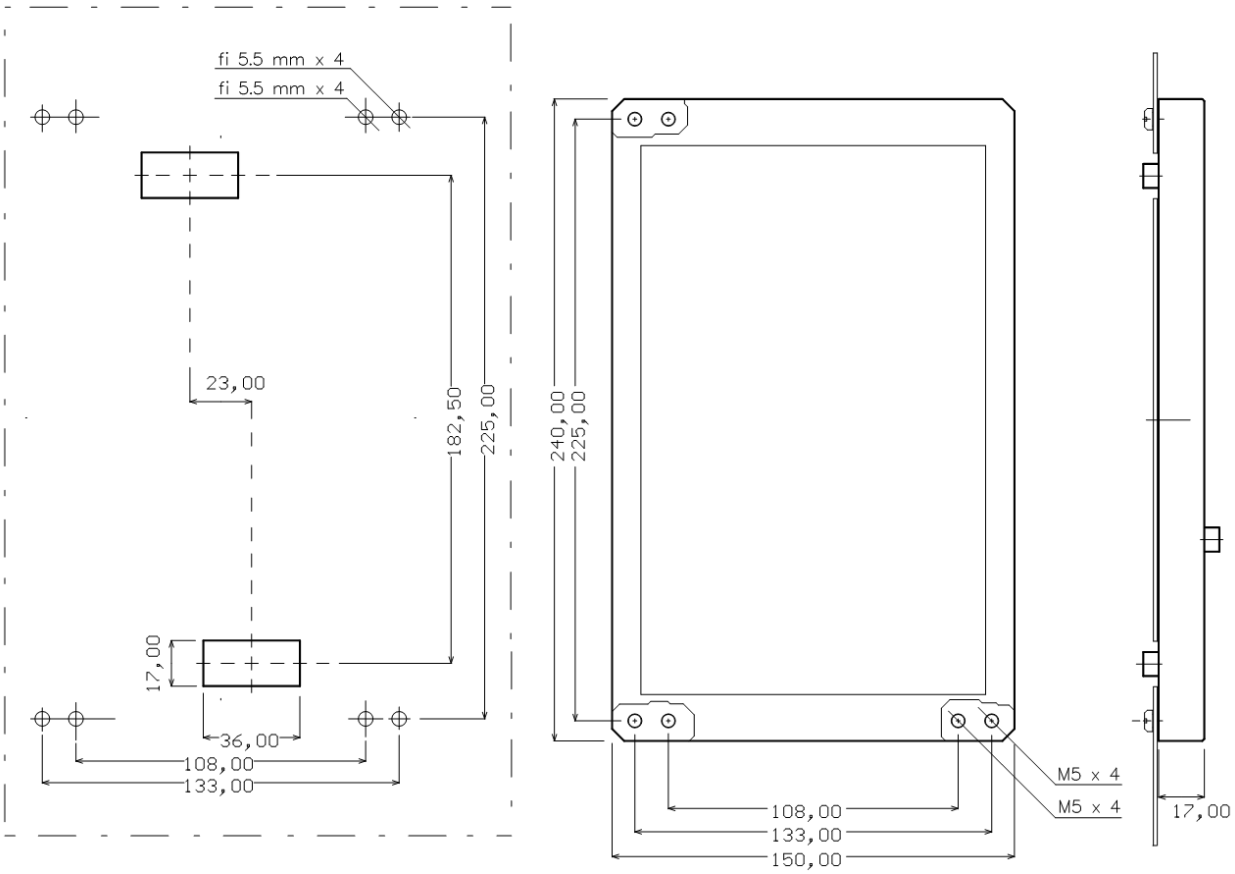
5. INSTALLATION DATA

- For **panel flush** installation **(7-slot enclosure)**.
  Mechanical installation for the **integrated panel** version.

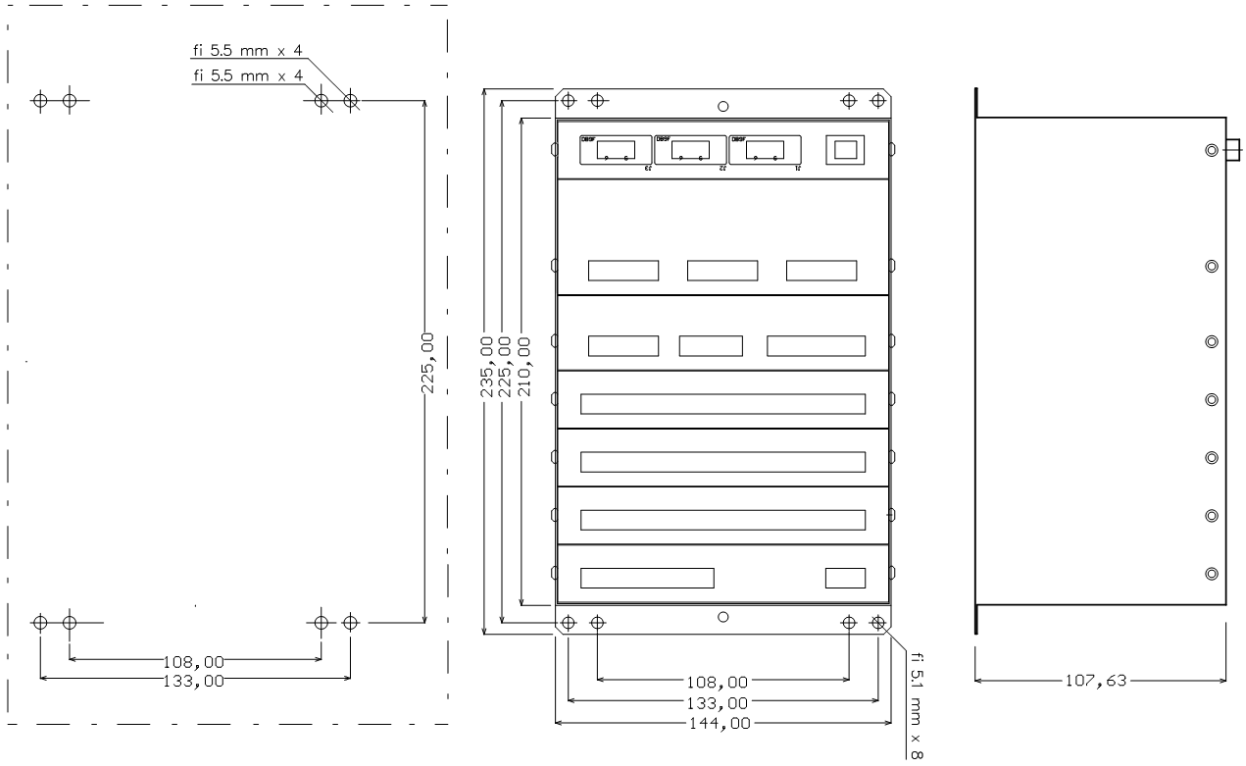


Drilling diagram.

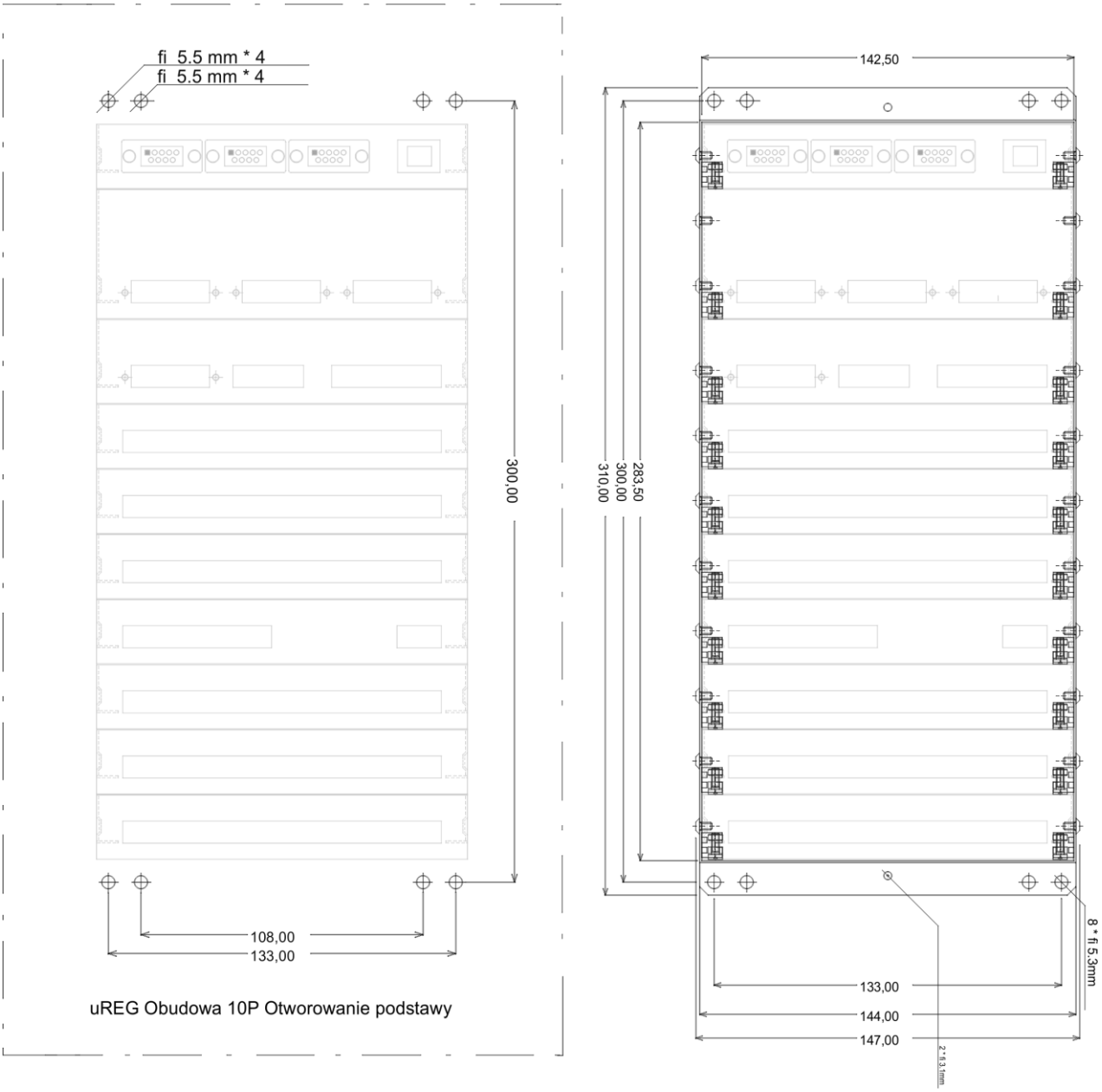
- **Panel flush (#2)** version.
  Mechanical installation for the **remote panel** version.



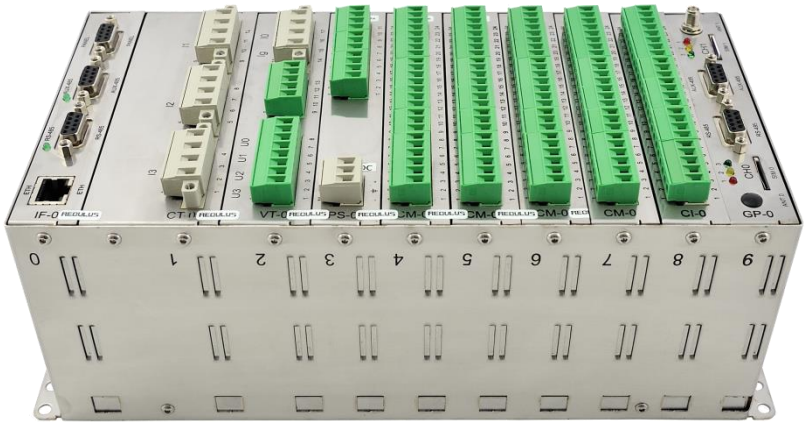
Drilling diagram for the panel.

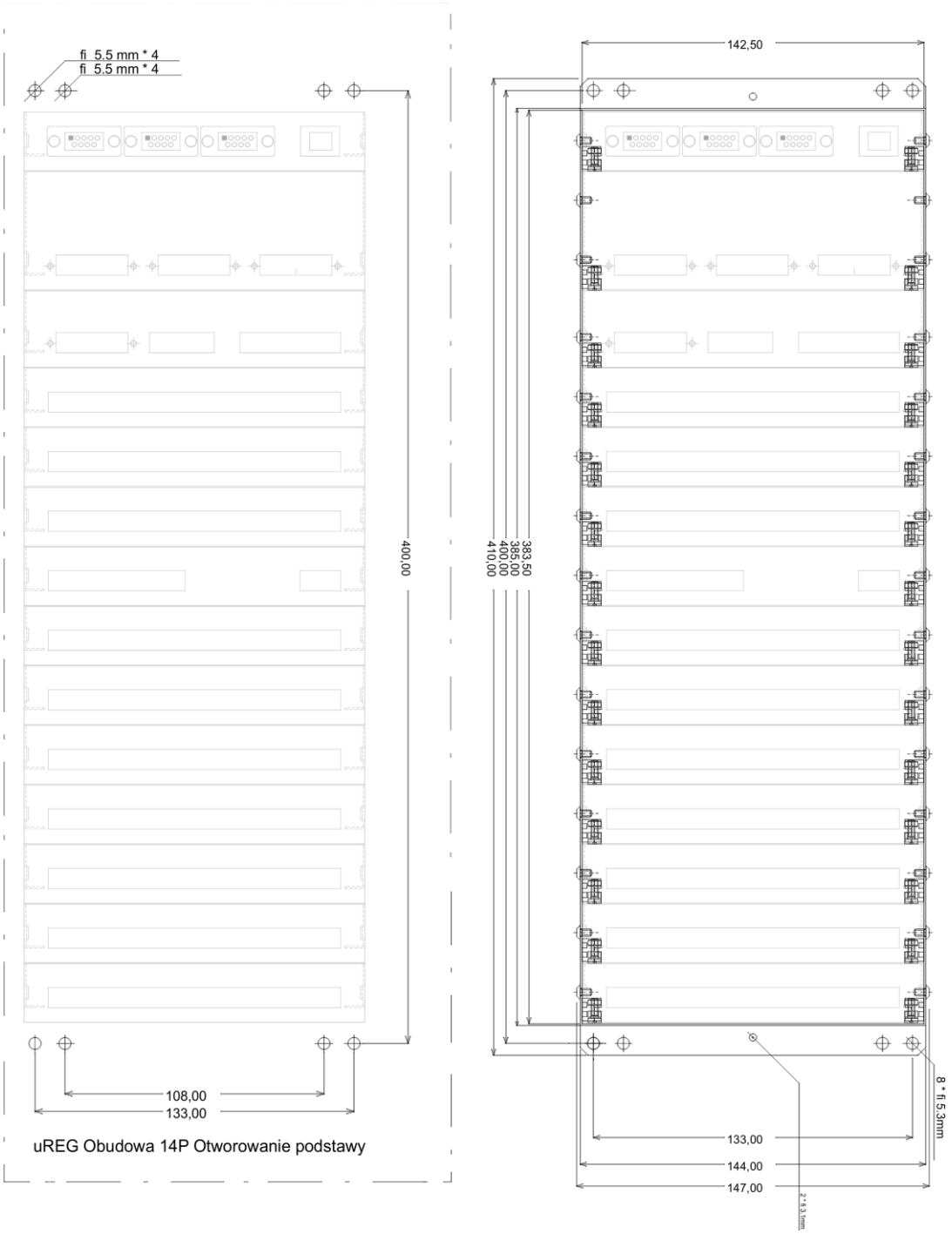


Drilling diagram for **7-slot** enclosure installation.



Drilling diagram for **10-slot** enclosure installation.

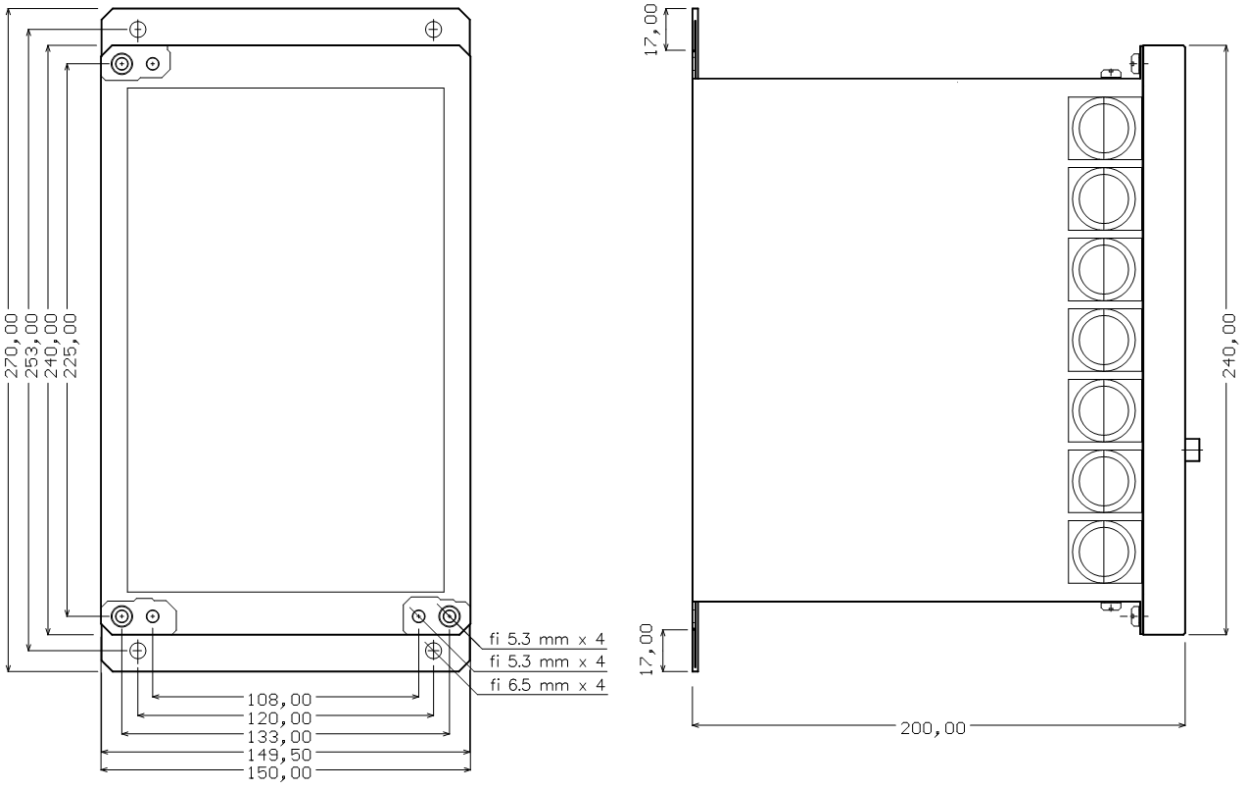




uREG Obudowa 14P Otworowanie podstawy

Drilling diagram for **14-slot** enclosure installation.

- For **panel surface** installation **(7-slot enclosure)**.
  Mechanical installation for the **integrated panel** version.



Drilling diagram.

REMARKS:

1. Prior to fastening the panel to the enclosure with an integrated panel, drive in UNC4-40 screws into DB9M sockets in the panel.
2. Alternatively, for a remote panel installation, drive in UNC4-40 screws in DB9M threaded openings to be able to screw on the connecting cable.
3. After completed device installation, the protective wrap on the LCD screen window can be removed.
4. Before applying auxiliary voltage, the device must be effectively earthed. For this purpose, use a sawtooth washer and a M5 screw to fasten the enclosure to the switchboard. Make sure the earthing conductor has the right cross-section (2.5 mm^2).

6. DESIGN AND STRUCTURE OF THE *u*REG SYSTEM

*u*REG system is modular. The modular design applies both to electronic hardware, used to assemble a specific device, but also to its enclosure and functional software. The device software has separate layers which carry out distinctly distinguished tasks.
*u*REG is fully reprogrammable (also remotely); the user is not required to interfere in device internals.

6.1. HARDWARE

Electronic circuits in the *u*REG system are divided into 3 groups:

- motherboard (**MB**) placed in the device enclosure;
- module boards arranged in slots on the motherboard;
- operator panel board (integrated, in remote configuration or optional).

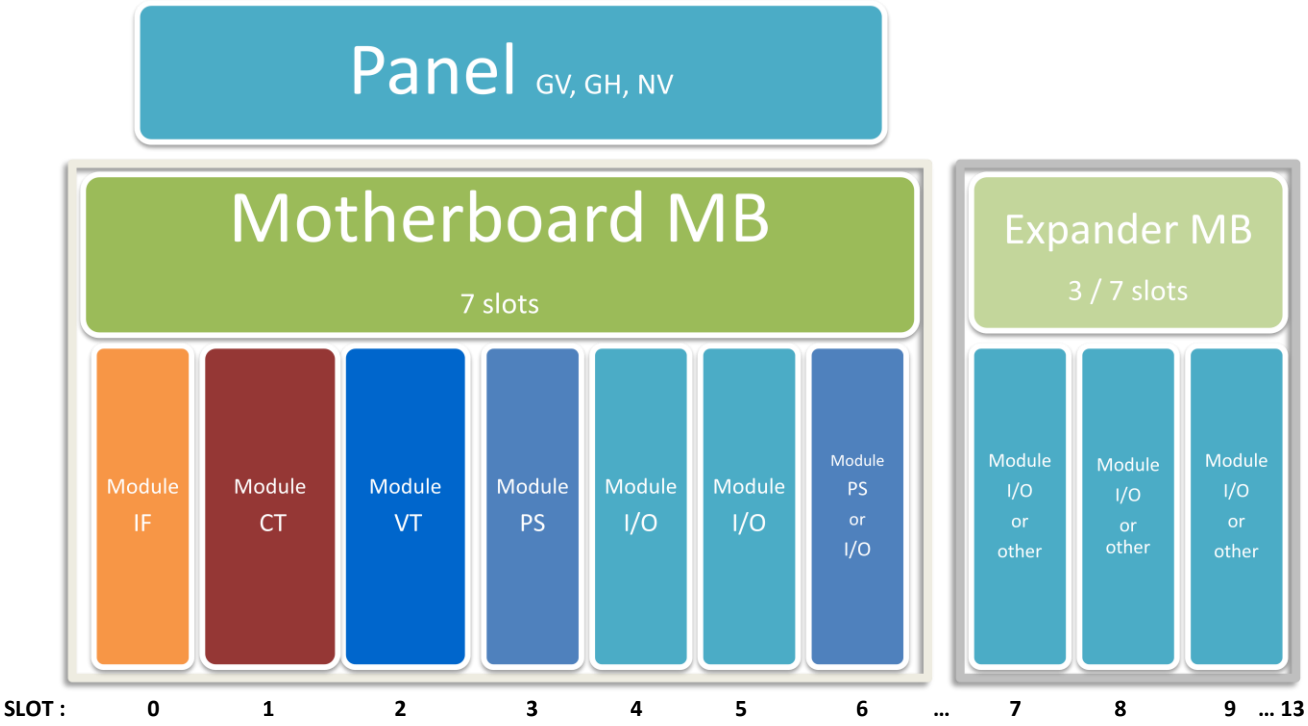


Fig. 6.1.1. Structure of *u*REG hardware.

The enclosure and the motherboard (**MB**) are equipped with **7 slots** numbered from 0 to 6 for module boards. In special design versions of the *u*REG unit, the mother board (**MB**) can be developed using **an expander** by **3 or 7 additional slots**.
Module slots on the motherboard are coded (and cannot be mistaken), i.e. their positions and sized determine their dedicated modules.

Mounting arrangement (mounted behind or in front of the panel) envisages 3 enclosure versions to be installed horizontally (H) or vertically (V). Small dimensions of the enclosure make it possible to place *u*REG modules practically in all commonly used chambers in MV and HV substations. Dimensions and installation data for all versions are shown in the figure in section **"Installation data"**.

Fig. 6.1.2. The 7-slot enclosure viewed on the side of module terminals (different configurations, enclosure mounted behind the panel).

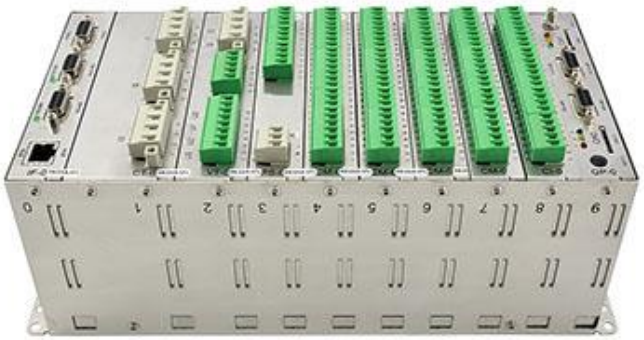


Fig. 6.1.3. The 10-slot enclosure viewed on the side of module terminals (enclosure mounted behind the panel).

The decision on numbers and types of applied modules is made by the user, depending on expected protective function to be provided by *u*REG. However, the minimum configuration must include:

- one computer-communication module of the **IF-x** main processor [**x=0,1,2,3,4**] (slot 0);
- one **PS-0** or **PS-1** switching-type power supply module, equipped with inputs, outputs and an alarm circuit (dedicated to slot 3 or 6).

In addition, the user can make use of the following modules:

- **CT-0** – IL1, IL2, IL3 current transformers module (dedicated to slot 1);
- **VP-0** – module for the third section of voltage transformers for ATS units;
- **VT-0, VT-5** – standard voltage and current (I0, Ig) transformers module with analogue inputs (dedicated to slot 2);
- **VT-1, VT-2** – module with double voltage transformers and I0 (dedicated to slot 2);
- **VT-3, VT-4, VT-8** – module with double voltage transformers and I1+I2+I3 (dedicated to slot 2);
- **VT-6** – voltage transformer module for the second current section as well as Ig and I0 (to slot 2);
- **VT-7** – module with 3 x 500 V AC voltage transformers and two full stars (If) (dedicated to slot 2);

and I/O modules dedicated to slots no. 3, 4, 5, 6, [7..13]:

- **CR-0, CM-0** – smart I/O modules with a power relay and inputs with programmable sensitivity threshold;
- **CO-0** – smart module with 16 relay outputs;
- **CI-0** – smart module with 16 inputs and one relay output;
- **IO-0** – universal digital input/output module, in particular with bidirectional inputs/outputs of programmable input resistance (220/24 V DC);
- **SS-0** – simplified I/O module with alarm circuit (dedicated to slot 3 or 6);
- **GP-0** – two-channel GPRS modem module;
- other modules (developed gradually).

All modules are automatically recognized and configured by the device in *Plug & Play mode*.

External terminal connectors and communication connectors (IF-x module) are accessible at the back of the enclosure. A detailed description of the modules is provided in section 7.

*u*REG can be equipped with one of three operator panels:

- **GH** panel – graphic color TFT LCD screen in QVGA standard, in horizontal arrangement;
- **GV** panel – graphic color TFT LCD screen in QVGA standard, in vertical arrangement;
- **NV** panel – with alphanumeric LCD, in portrait arrangement.

Each panel can be integrally front mounted, back mounted or mounted of the enclosure side. Alternatively, the panel can be installed remotely and wired.
All panels are equipped with dedicated fully programmable microcontrollers.

It is also possible for *u*REG to function without any operator panel installed. In this case it can be replaced by a virtual panel in software installed in an external (remote) PC.

6.2. SOFTWARE STRUCTURE

*u*REG is equipped with three computers which operate in parallel with precisely defined tasks.

- The computer on the motherboard (**MB**) executes measurements tasks and communication with modules.
- The **panel** computer provides communication with the operator (keyboard, display, LEDs, RS232 and USB links).
- Superior tasks of *u*REG system are executed by the main computer located on the **IF-x** module board; this computer's software has three separate layers with precisely defined functionalities.

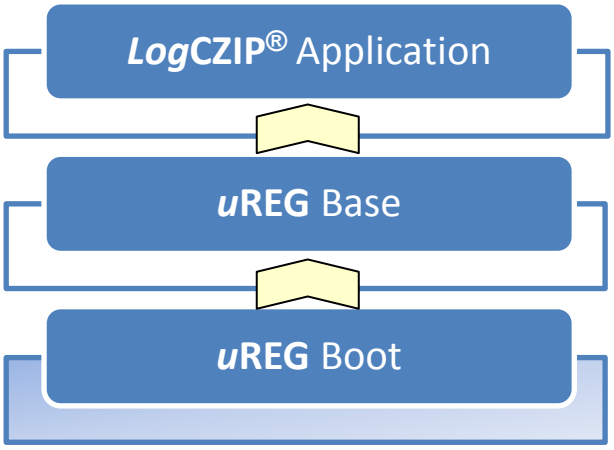


Fig. 6.2. Software structure

- **the lowest** layer (the so-called **BOOT**) – handles reprogramming all computers and initializing higher layers.

- **interlayer** (the so-called **BASE**) – is a real time operating system (RTOS), that executes communication between all internal computers (MB, panel), external communication (2 x RS-485/FO ports, Ethernet port, RS-232, USB) under several transmission protocols and executes **all criteria and fault protection tasks of the device according to rules defined within the top layer**, i.e. **APPLICATION**.

  The lowest layer (**BOOT**) and the interlayer (**BASE**) create **firmware** (embedded by the manufacturer) The user is still able to update **BASE.**

- **top** layer (the so-called **APPLICATION**) – is a structure consisting of logic conditions to decide on the purpose and protective functions provided by *u*REG.

  The **APPLICATION** layer is defined by the manufacturer or user via ***LogCZIP*** utility software. The **APPLICATION** layer is described in a separate operation manual.

7. *u*REG HARDWARE MODULES

All *u*REG system modules have standard external dimensions: 142.0 x 90.0 mm (width x height).

The modules are installed in respective slots on the motherboard (**MB**). Slot arrangement and sizes (IDC type) on the motherboard (**MB**) determine corresponding slots for the modules, which prevents making an error. All modules are unambiguously recognized and configured by the device, which takes place automatically in Plug & Play.

In terms of their design and functions, the modules can be divided into **two groups**:

1. dedicated to specific slots;
2. universal (dedicated to a range of slots).

Group 1 includes the following modules:

- **IF-0** / **IF-1** / **IF-2** / **IF-4** – ***i***nter***f***aces module for computer-communication purposes of the master processor, dedicated to slot **#0**;
- **CT-0** – ***c***urrent ***t***ransformers module dedicated to slot **#1**;
- **VP-0** – voltage transformers module dedicated to slot **#1**;
- **VT-0, VT-5** – ***v***oltage and current ***t***ransformers module, dedicated to slot **#2**;
- **VT-1, VT-2** – double ***v***oltage ***t***ransformers module with a current transformer (I0), dedic. to slot **#2**;
- **VT-3, VT-4, VT-8** – double ***v***oltage ***t***ransformers module (without U0) with current transformers (I1+I2+I3), dedicated to slot **#2**;
- **VT-6** – voltage transformers module, transformers of the second current section + Ig, I0 (dedicated to slot **#2**);
- **VT-7** – module with 3 x 500 V AC voltage transformers and two full stars (If) (dedicated to slot 2);
- **PS-0** / **PS-1** – ***p***ower ***s***upply module (switching-mode power unit), equipped with inputs, outputs and a circuit to handle alarms, dedicated to slot **#3 and/or #6**;
- **SS-0** – ***s***imple ***s***ervice module which is a simplified I/O module with an alarm support circuit (like **PS** but without power unit), dedicated to slot(s) **#3 and/or #6**.

Universal modules in **group 2** → dedicated to slots **3 to 6** [**7 to 13** for versions equipped with an expander]:

- **CR-0, CM-0, CI-0** – smart I/O modules (including those with power relays) and programmable sensitivity threshold inputs;
- **CO-0** – module with 16 relay outputs;
- **IO-0** – ***i***nput/***o***utput module with digital bidirectional inputs/outputs of programmable input resistance (220/24 V DC);
- **GP-0** – two-channel GPRS modem module, dedicated to slots **6 to 13**.

All *u*REG system modules (except **IF-x** and *GP-0*) are equipped with PhoenixContact Combicon and/or Wieland external strips (pitch: 7.50 and 5.00 mm).
The **CO-0** module is an exception; It has 32 terminals with the pitch of 3.50 mm.

The module slots can be used together with a wide range of pins (parallel, perpendicular, and slanted arrangement). With this solution, if necessary, **the entire unit can be replaced smoothly within interfering in terminal sheathing**.

The pins can have screw or spring terminals as well as measurement slots or pins for probes. For slots having more contacts, it is recommended to use pin stacks. The pin type and model are specified in the purchase order.

The description of terminals in *u*REG strictly depends on hardware configuration (modules) and logic of **APPLICATION**.

7.1. IF-0 / IF-4 MODULE (SLOT 0)

***I**nter**f**aces* module of ARM CPU, operating memory, settings memory, event reports and data recorder.

The **IF-0** module is equipped with the following connectors:

- **ETH** – magnetic insulation 8P8C port (i.e. RJ-45) of Ethernet 10/100BASE-T interface (TCP/UDP/ICMP protocols);
- **RS-485** – galvanic separation DB9F (female) port of RS-485 main interface w/ dedicated LED indicating interface activity; speed range: 300 to 512 000 Bd; full duplex (2 twisted pairs), distance up to 1000 m, up to 256 bus nodes;
- **AUX-485** – galvanic separation DB9F port of AUX-485 auxiliary interface w/ dedicated LED indicating interface activity; speed range: 300 to 512 000 Bd; full duplex (2 twisted pairs), distance up to 1000 m, up to 256 bus nodes;
- **PANEL** – 3 insulated DB9F ports of PN-485 interface to connect the operator panel; ports located at the top, side and bottom of the module; full duplex, distance 0 to 15 m;

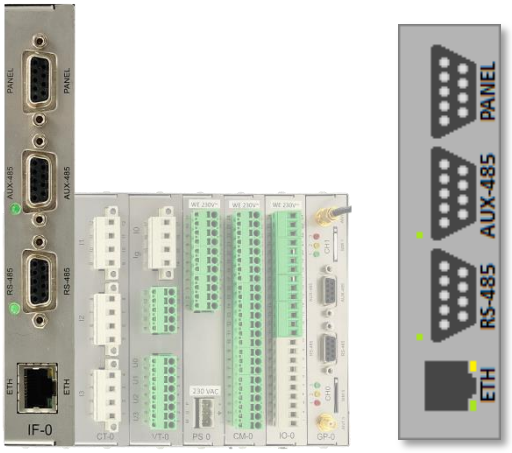


Fig. 7.1. Connectors of the IF-0 module.

Provided communication protocols:

- uCZIPstd (slave and master),
- uCZIPnet,
- DNP3.0,
- IEC 60870-5-103,
- IEC 60870-5-101/-104,
- IEEE-1588 (PTP time synchronization: precision = 1 µs),
- CZIPstd (slave and master, backward compatibility),
- CAN-PPM2 (for IF-3),
- Modbus ASCII,
- Modbus RTU (master and slave),
- Modbus TCP,
- Compatible with IEC-61850.

The **IF-x** module is required to start up *u*REG.

The **IF-4** module is a functional equivalent of IF-0, equipped with 2 x CAN-BUS interfaces.

The **IF-3** module – functional equivalent of IF-4, out of production.

7.2. IF-1 / IF-2 MODULE (SLOT 0)

Versions of the IF-0 module equipped with fiber optic (***FO*** – ***f***iber ***o***ptic) connectors (IF-1: one Tx-Rx pair or IF-2: two pairs) instead of copper RS-485 and AUX-485 interfaces.

Two fiber types are allowed:

- plastic fiber (POF diam. 1 mm, type 660 nm, FSMA, distance up to 60 m),

or

- glass fiber (GF 62.5/125 um, MM type 880 nm, ST, distance up to 1200 m).

Fig. 7.2. Connectors of the IF-1 / IF-2 module.

7.3. IF-4 MODULE (SLOT 0)

A new interface module providing a combined functionality of IF-0 and IF-3 modules; RS-485 and AUX-485 interfaces are compatible with CAN-BUS.

In addition, the **IF-4** module is equipped with new expanded memory units (8 or 16 MB: to be specified in the purchase order) to provide a wider range of buffer configuration and (combined with the MB-2 / MB-3 motherboard module) **sampling mode at 3200 Hz** (64 samples per period). Details → see chapter 15.

7.4. CT-0 MODULE (SLOT 1)

In the **CT-0** module (***c***urrent ***t***ransformers module), there are 3 current transformers for direct measurements of phase currents within the range (In: 5 A, 1 A) = 0 ÷ 192 A.

Phase current input circuits

Rated current In	5 A or 1A
Measurement range	0 ÷ 192 A
Measurement error within ranges:	0.05 ÷ 0.35 A <5 %
	0.35 ÷ 50 A <1.5 %
	50 ÷ 192 A <5 %
Power input at I=In	<0.5 VA
Rated frequency fn	50 Hz
Continuous current-carrying capacity	3 * In
1-second thermal endurance	100 * In
Dynamic withstand value	250 * In

Terminals of the **CT-0** module are grouped into three Wieland-Wiecon 4-pin symmetric ports (screwed, type 8313S/4 WF OB; pitch: 7.50 mm, max continuous capacity 12 A, 400 V, cable cross-section 2.5 mm2). Each pin k, l on the transformers is connected to two connector terminals.

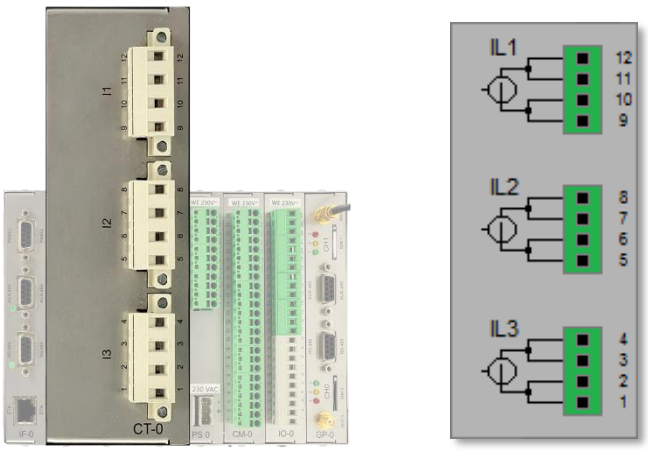


Fig. 7.4. Terminals of the CT-0 module.

The **CT-0** module is required for fulfillment of the following protective criteria, e.g.:

- Overcurrent I>
- Tripped overcurrent I>T
- Overcurrent dependent I>
- Undercurrent
- I0> (vector sum of currents Ir, Is, It)
- Current asymmetry aI>
- I>tilt (polygonal characteristic curve)
- I1>, I2>, I3> for MSK.

7.5. VP-0 MODULE (SLOT 1)

VP-0 – module in the third voltage section, e.g. ATS units.

Terminals of the **VP-0** module are grouped into three Wieland-Wiecon 4-pin symmetric ports (screwed, type 8313S/4 WF OB; pitch: 7.50 mm, max continuous capacity 12 A, 400 V, cable cross-section 2.5 mm2).

Each pin on the transformers is connected to two connector terminals.

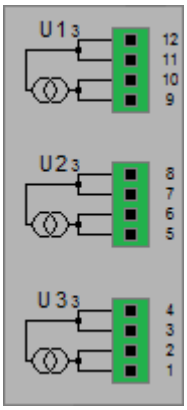


Fig. 7.5. Terminals of the VP-0 module.

7.6. VT-0 / VT-5 MODULE (SLOT 2)

The ***VT-0*** module houses 4 measuring voltage transformers for U0, U1, U2, U3 and 2 current transformers for I0 and Ig. The module additionally has 3 unipolar digital inputs (AUXI 0..2), which can be also used for analogue measurements (sensitivity threshold selectable by setting).

Terminals of the **VT-0** module are grouped into 3 x Phoenix-Contact/Wieland slots:

- 8-pin MSTBA2.5/8-G strip (pitch: 5.00 mm, max 12 A, 250 V)
  for measurement of **U0, U1, U2, U3** voltages within the range (Un: 100 V) = 0 ÷ 130 V;
- 5-pin MSTBA2.5/5-G strip (pitch: 5.00 mm, max 12 A, 250 V)
  for **AUXI0, AUXI1, AUXI2** inputs = 0 ÷ 130 V;
- 4-pin GMSTBA2.5/4-G strip (pitch: 7.50 mm, max 12 A, 400 V)
  for measurement of currents **I0, Ig** within the range (In: 1 A) = 0 ÷ 10 A.

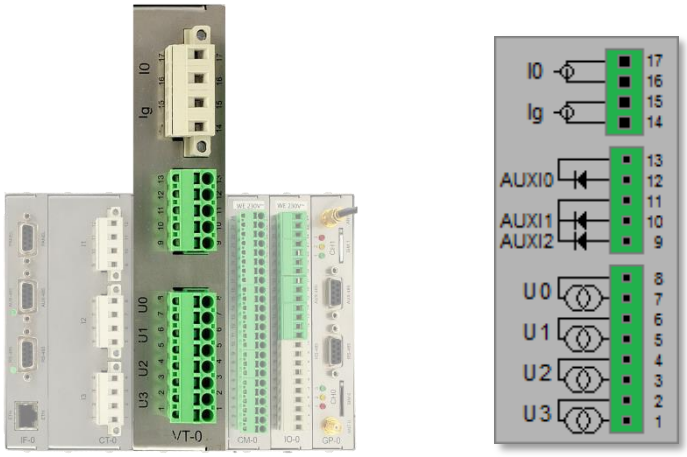


Fig. 7.6. Terminals of the VT-0 module.

The **VT-0** module (combined with **CT-0**) is required for fulfillment of the following protective criteria and functions, e.g.:

- Overvoltage U>
- Tripped overvoltage U>T
- Overvoltage U0>
- Undervoltage U<
- Tripped undervoltage U<T
- Frequency
- Frequency derivative df/dt>
- Second harmonic f100Hz>
- AWSCz automatic unit controller
- U1>, U2>, U3> for MSK
- Internal fSPZ/SCO
- Overcurrent earth-fault criterion I0>
- Overcurrent Ig>
- Susceptance B0kier.>
- Conductance G0>
- Admittance Y0>
- Admittance YY0>
- Overpower for 3-phase reactive power (1 min.) Q3f>
- Overpower for 3-phase active power (1 min.) P3f>
- Undervoltage U< (polygonal characteristic curve)
- Single-phase undervoltage U<
- Power directional
- Vector Shift
- capacitor bank /BKR/ control
- Resistor controller
- Directional overcurrent earth-fault I0k>
- Conductance G0>kier.
- Underpower for 3-phase reactive power (1 min.) Q3f<
- Underpower for 3-phase active power (1 min.) P3f<

The **VT-5** module is identical in terms of functionality, but it features increased measurement threshold for voltages **U0, U1, U2, U3** within the range **5 – 260 V (optionally 500 V AC)**.

7.7. VT-2 / VT-1 MODULE (SLOT 2)

The **VT-2** module with double *v*oltage ***t***ransformers is mainly designed for supporting ATS automatic units and wind plants.
The **VT-2** module houses 2 sets of 4 measuring transformers for voltages U0, U1, U2, U3 and 1 current transformer for I0.

Terminals of the **VT-2** module are grouped into 3 x Phoenix-Contact/Wieland slots:

- 8-pin MSTBA2.5/8-G strip (pitch: 5.00 mm, max 12 A, 250 V) for measurement of **U0, U1, U2, U3** voltages in section 1 within the range (Un: 100 V) = 0 ÷ 130V;
- 8-pin MSTBA2.5/8-G strip (pitch: 5.00 mm, max 12 A, 250 V) for measurement of **U0, U1, U2, U3** voltages in section 2 within the range (Un: 100 V) = 0 ÷ 130V;
- 2-pin GMSTBA2.5/2-G strip (pitch: 7.50 mm, max 12 A, 400 V) for measurement of current **I0** within the range (In: 1 A) = 0 ÷ 10 A.

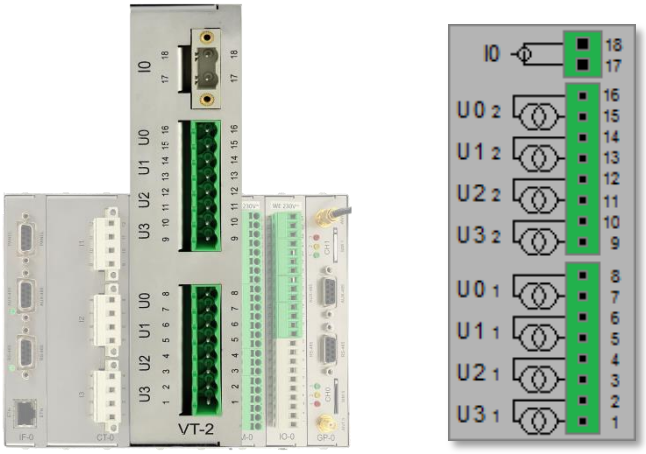


Fig. 7.7. Terminals of the VT-2 module.

The **VT-2** module (combined with **CT-0**) is required for fulfillment of the following protective criteria and functions, e.g.:

- Overvoltage U> [in Section 1 and 2]
- Tripped overvoltage U>T [in Section 1 and 2]
- Overvoltage U0> [in Section 1 and 2]
- Undervoltage U< [in Section 1 and 2]
- Undervoltage U<T [in Section 1 and 2]
- Difference of sectional voltages [1-2]
- Frequency [in Section 1 and 2]
- Frequency derivative df/dt>
- Vector Shift
- Voltage derivative dU/dt
- Second harmonic f100Hz>
- BKR capacitor bank control
- AWSCz automatic unit controller
- Synchro-check on both sections
- deltaf< [Section 1-2]
- Power directional
- Internal fSPZ/SCO
- Overcurrent earth-fault criterion I0>
- Susceptance B0kier.>
- Conductance G0>
- Conductance G0>kier.
- Admittance Y0>
- Admittance YY0>
- Underpower for 3-phase reactive power (1 min.) Q3f<
- Overpower for 3-phase reactive power (1 min.) Q3f>
- Underpower for 3-phase active power (1 min.) P3f<
- Overpower for 3-phase active power (1 min.) P3f>
- Resistor controller

The **VT-1** module is identical in terms of functionality, but it features increased measurement threshold for voltages **U0, U1, U2, U3** within the range **5 – 260 V (optionally 500 V AC)**.

7.8. VT-3 / VT-4 / VT-8 MODULE (SLOT #2)

The **VT-3** module with double *v*oltage ***t***ransformers is mainly designed for supporting automation solutions at wind plants.

The **VT-3** module houses 2 sets of 4 measuring transformers for voltages U1, U2, U3 and 3 current transformer for If.

Terminals of the **VT-3** module are grouped into 3 x Phoenix-Contact/Wieland slots:

- 6-pin MSTBA2.5/6-G strip (pitch: 5.00 mm, max 12 A, 250 V) for measurement of **U0, U1, U2, U3** voltages in section 1 within the range (Un: 100 V) = 0 ÷ 130V;
- 6-pin MSTBA2.5/6-G strip (pitch: 5.00 mm, max 12 A, 250 V) for measurement of **U0, U1, U2, U3** voltages in section 2 within the range (Un: 100 V) = 0 ÷ 130V;
- 6-pin GMSTBA2.5/6-G strip (pitch: 5.00 mm, max 12 A, 400 V) for measurement of current **If** within the range (In: 1 A) = 0 ÷ 10 A.

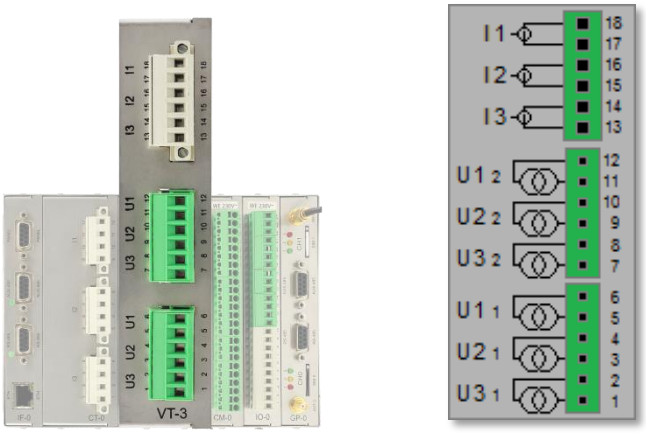


Fig. 7.8. Terminals of the VT-3 module.

The **VT-3** module (combined with **CT-0**) is required for fulfillment of the following protective criteria and functions:

- Overvoltage U> [in Section 1 and 2]
- Tripped overvoltage U>T [in Section 1 and 2]
- Overcurrent earth-fault criterion I>
- Undervoltage U< [in Section 1 and 2]
- Undervoltage U<T [in Section 1 and 2]
- Difference of sectional voltages [1-2]
- Frequency [in Section 1 and 2]
- Frequency derivative df/dt>
- Voltage derivative dU/dt
- Second harmonic f100Hz>
- BKR capacitor bank control
- AWSCz automatic unit controller
- Synchro-check on both sections
- deltaf< [Section 1-2]
- Power directional
- Internal fSPZ/SCO
- Susceptance B0kier.>
- Conductance G0>
- Conductance G0>kier.
- Admittance Y0>
- Admittance YY0>
- Overpower for 3-phase reactive power (1 min.) Q3f>
- Underpower for 3-phase reactive power (1 min.) Q3f<

The **VT-4** module is identical in terms of functionality, but it features increased measurement threshold for voltages **U1, U2, U3** within the range **5 – 260 V (optionally 500 V AC)**.

The **VT-8** module is a functional equivalent to the **VT-4** module; additionally, it has **current transformers for rated current In = 5 A**.

7.9. VT-6 MODULE (SLOT #2)

VT-6 – voltage transformers module, transformers of the second current section + Ig, I0.

Under development.

7.10. VT-7 MODULE (SLOT #2)

The module has three voltage transformers for **U1, U2, U3** within the range **5 ÷ 260 V (optionally 500 V AC)** and **two full If stars.**

Terminals on the **VT-7** module are grouped into 3 x Wieland slots:

- 6-pin MSTBA2.5/6-G strip (pitch: 5.00 mm, max 12 A, 250 V)
  for measurement of **U1, U2, U3** voltages in section 1 within the range (Un: 230 V) = 0 ÷ 500 V;
- 6-pin GMSTBA2.5/6-G strip (pitch: 5.00 mm, max 12 A, 400 V)
  for measurement of current **If in section 2** within the range (In: 1 A) = 0 ÷ 10 A.
- 6-pin GMSTBA2.5/6-G strip (pitch: 5.00 mm, max 12 A, 400 V)
  for measurement of current **If in section 3** within the range (In: 1 A) = 0 ÷ 10 A.

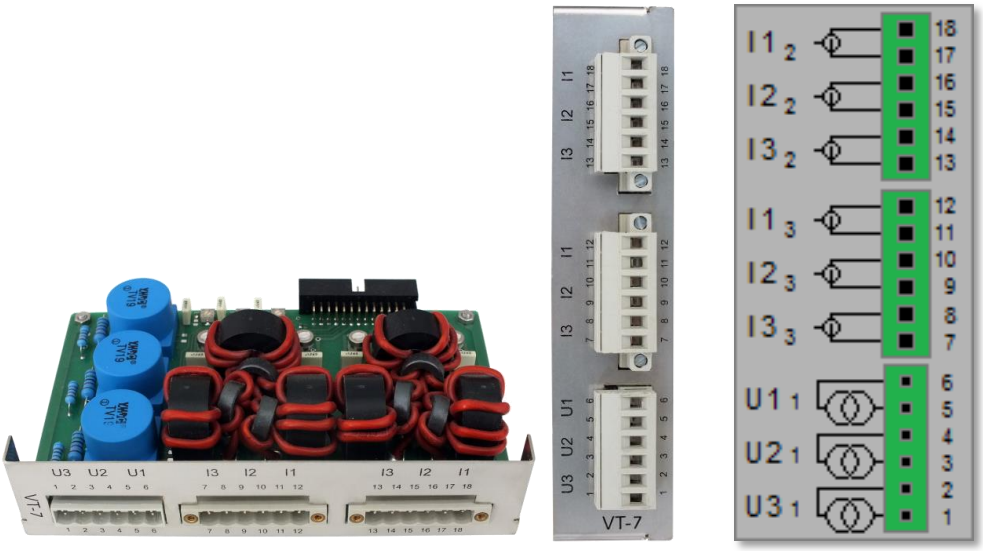


Fig. 7.10. Terminals of the VT-7 module.

7.11. PS -0/ SS-0 MODULE (SLOTS 3 & 6)

The **PS-0** ***p***ower ***s***upply module is a switching power unit module dedicated to *u*REG. Each *u*REG unit can be equipped with one or two PS-0 module(s) (installed in slot #3 and/or #6). For a configuration with two PS-0 modules, each of them can be powered by separate guaranteed voltage (the other module serves as "hot standby").

Rated supply voltage	220 V DC (or 230 V AC)
Admissible range of supply voltage changes: AC	88 ÷ 365 VDC (100 ÷ 260VAC)
Power input at 220 V DC	<15 W (type 7W)
Undervoltage protective interlock threshold:	> 375 V DC
Overvoltage interlock hysteresis:	app. 12 VDC

In addition, the PS-0 module is equipped with:

- 3 unipolar digital inputs → terminals 8, 9, 10;
- 2 make-contact relays (1 pair) → terminals 5, 6;
- switchable relay for handling the Alarm circuit → terminals 2, 3, 4;
- internal input of power unit efficiency control;

and (optionally)

- switchable relay for resetting the Alarm circuit (by means of an external contact-type logic system) → terminal 1

Terminals on the **PS-0** module are grouped into 2 slots:

- 3-pin MSTBA2.5/3-G strip (pitch: 5.00 mm, max 12 A, 250 V) to apply auxiliary supply voltage and earthing;
- 11-pin MSTBA2.5/11-G strip (pitch: 5.00 mm, max 12 A, 250 V) to handle inputs/outputs.

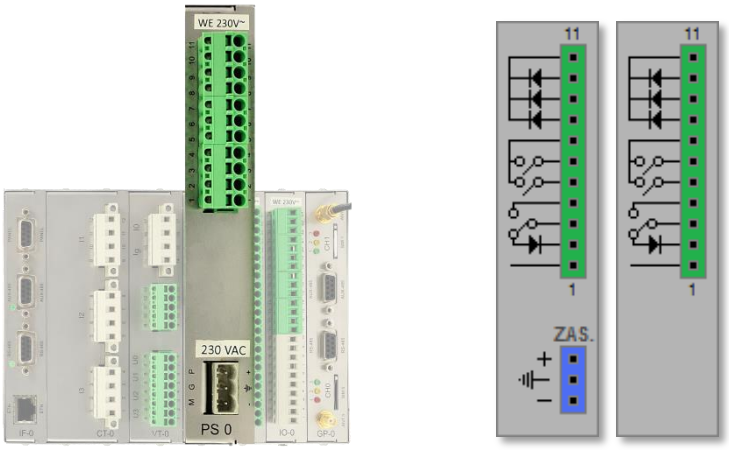


Fig. 7.11. Terminals of the PS-0 / SS-0 module.

CAUTION

For double power unit configurations (with hot standby), it is forbidden to replace the power unit module during operation of the device! In order to replace a faulty module, disconnect auxiliary power completely for the time of this action.

RECOMMENDATION

In order to maintain uniform equipment for different substations, it is always recommended to use a PS module relay (associated with terminals 2, 3 and 4) to signal the Alarm state. This relay can be used with both topologies applied to the AL circuit: serial and parallel.

For the serial topology, AL signaling is activated by opening the normally closed circuit. Thus, terminals #3 and #4 of the module must be connected to the series circuit. Terminal #3 should be connected up on the side of positive potential of the voltage source (usually +AwUp).

For the parallel topology, signaling is prompted by shorting the normally open circuit. This task is performed by a pair of contacts connected with terminals #2 and #3, wherein terminal #3 must be connected to the circuitous busbar to the positive potential (usually +AwUp; there is a silicon diode to polarize the circuit by a cathode along the route of terminals #2 and #3).
Once the negative potential (relative to the potential of terminal #3) is applied, terminal #1 provides effective exclusion of faulty or non-supplied *uREG* from the signaling circuit and restoration of Alarm bus readiness.

The **SS-0** module is a functional equivalent to the PS-0 module; it has no switching-mode power unit.

7.12. PS -1 MODULE (SLOTS 3 & 6)

The **PS-1** is a **24 V DC** switching power unit module dedicated to *u*REG.

Rated supply voltage:	24 V DC
Admissible range of supply voltage changes:	21 ÷ 38 V DC
Power input at 24 V DC	<15 W (type 7W)
Undervoltage protective interlock threshold:	none

Other parameters → see PS-0.

7.13. CR-0 MODULE (SLOTS 3 to 13…)

The **CR-0** module (controlled by a dedicated Cortex controller) is an universal I/O module with a power relay, equipped with:

- 2 x SR6-51 power relays → terminals 22, 24;
- 2 internal inputs for power relay control;
- 1+3+5 = 9 digital inputs with programmable sensitivity threshold >20/>50 V DC → terminals 1÷5, 13÷15, 17;
- 4 make-contact relays (2 pairs) → terminals 7, 8, 10, 11;
- 1 switchable relay → terminal 20.

All signals of CR-0/CM-0/PR-0/IO-0 modules are grouped into one 24-pin MSTBA2.5/24-G strip (pitch: 5.00 mm, max 12 A, 250 V).

CAUTION:

The strips can have pins with screw or spring terminals as well as measurement pins for probes. For 24-pin I/O modules, it is recommended to use pin stacks!

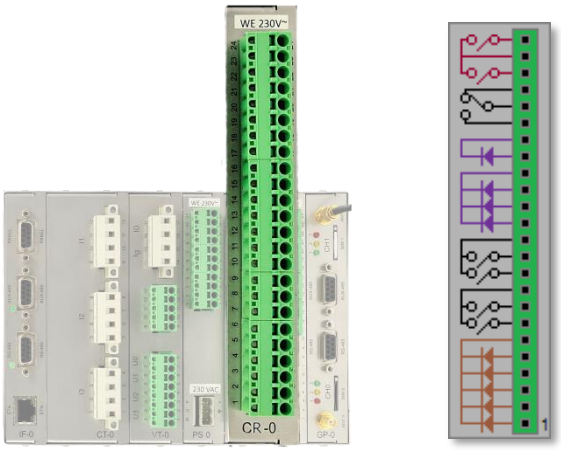


Fig. 7.13. Terminals of the CR-0 module.

CAUTION

Following a switching operation, a small electric charge Q of approx. 1.2 uC (microcoulombs) may persist on terminals 22 – 23 and/or 24 – 23.
Touching these terminal pairs may result in an unpleasant shock pulse.

7.14. CM-0 MODULE (SLOTS 3 to 13…)

CM-0 is analogous to CR-0; it features a less advanced configuration:

- 2 x SR6-51 power relays → terminals 22, 24;
- 2 internal inputs for power relay control;
- 1+1+4+5 = 11 digital inputs with programmable sensitivity threshold >20/>50 V DC → terminals 1÷5, 10÷13, 15, 17;
- 2 make-contact relays (1 pair) → terminal 7, 8;
- 1 switchable relay → terminal 20.

CAUTION:

The strips can have pins with screw or spring terminals as well as measurement pins for probes. For 24-pin I/O modules, it is recommended to use pin stacks!

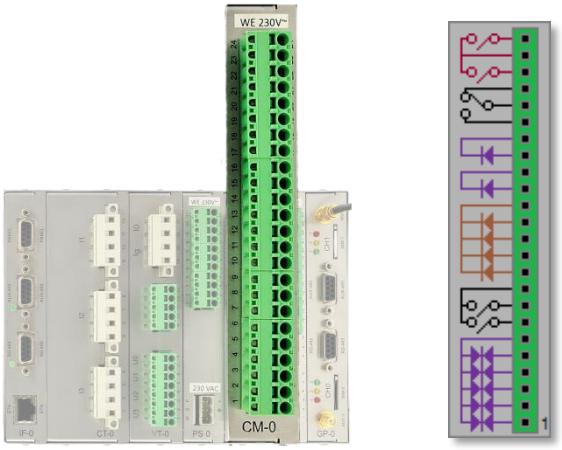


Fig. 7.14. Terminals of the CM-0 module.

CAUTION

Following a switching operation, a small electric charge Q of approx. 1.2 uC (microcoulombs) may persist on terminals 22 – 23 and/or 24 – 23.
Touching these terminal pairs may result in an unpleasant shock pulse.

7.15. CO-0 MODULE (SLOTS 3 to 13…)

The **CO-0** module is a smart module with 16 identical relay outputs (for signaling).

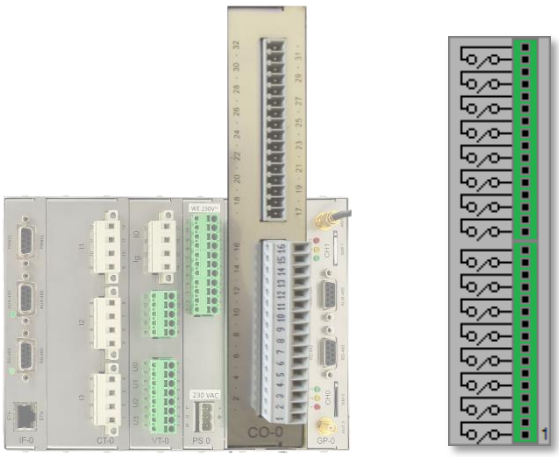


Fig. 7.15. Terminals of the CO-0 module.

7.16. CI-0 MODULE (SLOTS 3 to 13…)

CI-0 is a smart module with 16 digital inputs and 1 relay output (for signaling), with the following topology:

- 4+3 = 7 digital inputs with programmable sensitivity threshold >20/>50 V DC → terminals 1÷4, 10÷12;
- 3+2 = 5 unipolar digital inputs → terminals 6÷8, 14÷15;
- 2+2 = 4 bipolar digital inputs with programmable input resistance (220/24 V DC) → terminals 17÷18, 20÷21;
- 1 make-contact relay → terminal 23;

CAUTION:
The strips can have pins with screw or spring terminals as well as measurement pins for probes. For 24-pin I/O modules, it is recommended to use pin stacks!

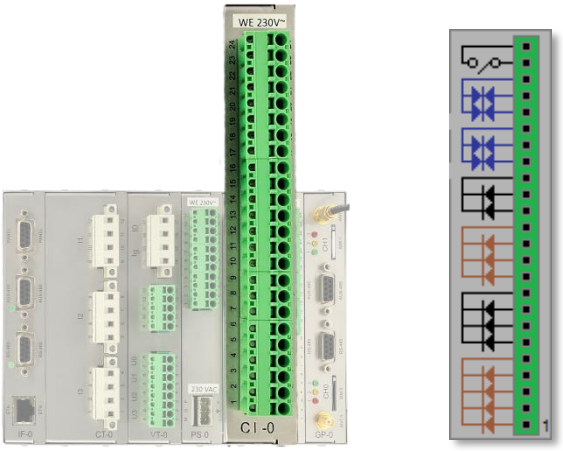


Fig. 7.16. Terminals of the CI-0 module.

7.17. IO-0 MODULE (SLOTS 3 to 13…)

The ***IO-0*** module is a universal digital input/output module, e.g. with programmable bidirectional inputs, equipped with:

- 2+3 = 5 bipolar digital inputs with programmable input resistance (220/24 V DC) → terminals 11÷13, 15÷16;
- 2+3 = 5 unipolar digital inputs → terminals 18÷20, 22÷23;
- 5 independent make-contact relays → terminals 1, 3, 5, 7, 9.

CAUTION:
The strips can have pins with screw or spring terminals as well as measurement pins for probes. For 24-pin I/O modules, it is recommended to use pin stacks!

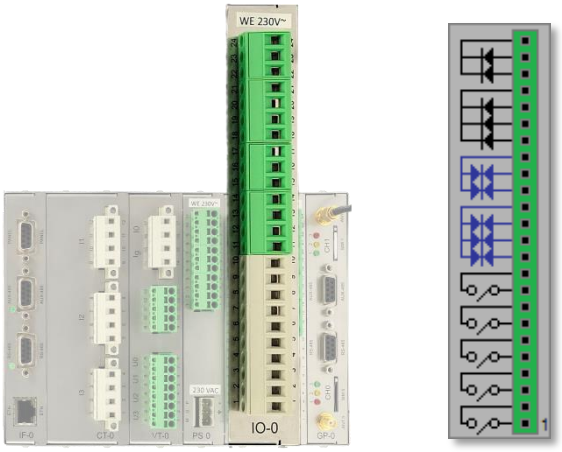


Fig. 7.17. Terminals of the IO-0 module.

7.18. GP-0 MODULE (SLOTS 6 to 13…)

GP-0 is a module of the internal double-channel ***GPRS*** modem for remote communication with *u*REG via ***GSM***.

- Features of the **GP-0** module:

- module form a wide range of uREG modules, installed in the protection slot (also supplied by the slot);
- SIM slot, push-push type (easy access to SIM);
- communications ports: 2 x RS-485, USB;
- SMA type antenna slots;
- signaling LEDs (3 per channel: GPRS for transmission + 2 programmable);
- configuration via WWW browser or *Monitor3*;
- full support for *prepaid* SIM cards (cost analysis, etc.);
- operated via phone (SMS notification), tablet, laptop/PC.

- Advantages of the solution:

- cost reduction: no need to use any additional communication equipment and external power units;
- guaranteed dependability: no need to arrange functional and protocol compatibility for devices supplied by different manufacturers;

- For use in:

- wind farms;
- biogas plants and photovoltaics;
- hydroelectric power stations;;
- small power supply stations, etc.

- Available versions:

- **GP-0/1** – single-channel (1 x SIM slot);
- **GP-0/2** – two-channel (2 x SIM slots);
- **GP-0/2/GPS** – two-channel (2 x SIM slots) w/ GPS receiver;
- **GP-0/x/z** – single or two-channel, external enclosure (supply: 12 V DC).

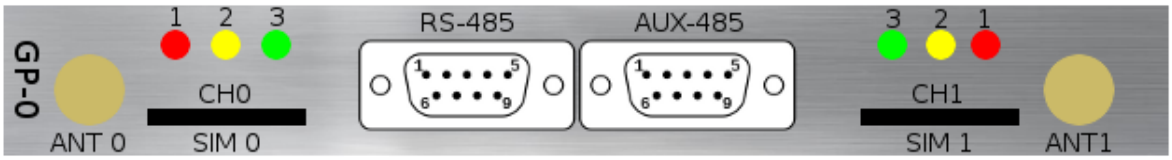
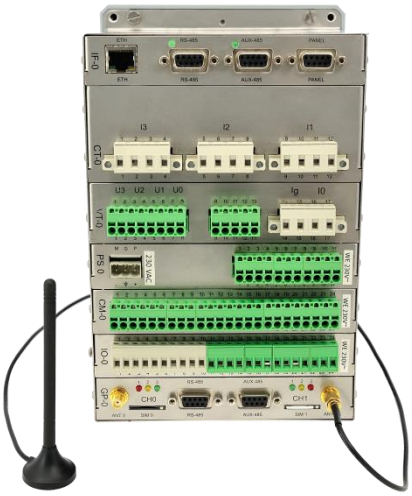


Fig. 7.18.1. Sockets of the GP-0 module.



Rys.7.18.2. *u*REG with the GP-0 module installed.

Full specification of the GP-0 module together with a presentation brochure are provided in a separate document.

7.19. FIXED HARDWARE CONFIGURATIONS

To facilitate distinction and specification of equipment, there are designations of fixed module combinations and slot arrangement in the enclosure, referred to as **hardware configurations** of *u*REG.

The most popular hardware configurations are presented in the following table.

Configuration \ Slot:	0	1	2	3	4	5	6	7	8	9
uREG-0	IF-x	CT-0	VT-0	PS-x	CM-0					
uREG-1	IF-x	CT-0	VT-0	PS-x	CM-0	IO-0				
uREG-2	IF-x		VT-2	PS-x	CM-0	CM-0				
uREG-3	IF-x	CT-0	VT-0	PS-x	CM-0	IO-0	CR-0			
uREG-4	IF-x	CT-0	VT-0	PS-x	CM-0	IO-0	CM-0			
uREG-5	IF-x	CT-0	VT-2	PS-x	CM-0	IO-0				
uREG-6	IF-x		VT-2	PS-x	CM-0	CM-0	IO-0			
uREG-7	IF-x	CT-0	VT-0	PS-x	CR-0	IO-0				
uREG-8	IF-x	CT-0	VT-2	PS-x	CM-0					
uREG-9	IF-x	CT-0	VT-0	PS-x	CM-0	CM-0	CM-0			
uREG-10	IF-x	CT-0	VT-0	PS-x	CM-0	IO-0	IO-0			
uREG-11	IF-x		VT-2	PS-x	CM-0	CM-0	CO-0			
uREG-12	IF-x	VP-0	VT-2	PS-x	CM-0	CM-0	CM-0			
uREG-13	IF-x		VT-2	PS-x	CM-0	CM-0	CM-0			
uREG-14	IF-x	CT-0	VT-0	PS-x	CM-0	CI-0				
uREG-15	IF-x		VT-2	PS-x	CR-0	CR-0				
uREG-16	IF-x	CT-0	VT-0	PS-x	CM-0	CI-0	CM-0			
uREG-17	IF-x		VT-0	PS-x	CM-0	IO-0				
uREG-18	IF-x	CT-0	VT-0	PS-x	CM-0	CI-0	CI-0			
uREG-19	IF-x	CT-0	VT-2	PS-x	CM-0	CI-0				
uREG-20	IF-x			PS-x						
uREG-21	IF-x	CT-0	VT-0	PS-x	CM-0	CM-0				
uREG-22	IF-x	CT-0	VT-3	PS-x	CM-0	CM-0	CM-0	CM-0	CM-0	
uREG-23	IF-x	CT-0	VT-0	PS-x	CM-0	CM-0	CM-0			
uREG-24	IF-x	CT-0	VT-3	PS-x	CM-0	CM-0				
uREG-25	IF-x	CT-0	VT-0	PS-x	CR-0	CI-0				
uREG-26	IF-x	CT-0	VT-0	PS-x	CR-0	CR-0	CR-0			
uREG-27	IF-x	CT-0	VT-2	PS-x	CR-0	CR-0	CR-0			
uREG-28	IF-x	CT-0	VT-3	PS-x	CM-0	CI-0				
uREG-29	IF-x	CT-0	VT-3	PS-x	CM-0	CM-0	CM-0	CM-0	CI-0	
uREG-30	IF-x	CT-0	VT-1	PS-x	CM-0	CM-0	CM-0			
uREG-31	IF-x	CT-0	VT-1	PS-x	CM-0	CM-0				
uREG-32	IF-x	CT-0	VT-2	PS-x	CM-0	CM-0				
uREG-33	IF-x		VT-0	PS-x	CM-0					
uREG-34	IF-x	CT-0	VT-4	PS-x	CM-0	IO-0				
uREG-35	IF-x	CT-0	VT-4	PS-x	CM-0	CM-0				
uREG-36	IF-x	CT-0	VT-0	PS-x	CR-0	CR-0	CI-0			
uREG-37	IF-x	CT-0	VT-2	PS-x	CR-0	CM-0	CR-0	CM-0	CM-0	CI-0
…										
uREG-50	IF-x		VT-0	PS-x						
uREG-51	IF-x	CT-0	VT-0	PS-x						
uREG-52	IF-x		VT-4	PS-x						
uREG-53	IF-x		VT-4	PS-x	CM-0					

Table 7.1. uREG configurations

8. OPERATOR PANEL – FRONT PANEL

According to section **6.1. Hardware**, *u*REG can be equipped with one of 3 operator panels:

- **GH** panel – color graphic LCD in TFT QVGA standard,
  in **horizontal** arrangement;

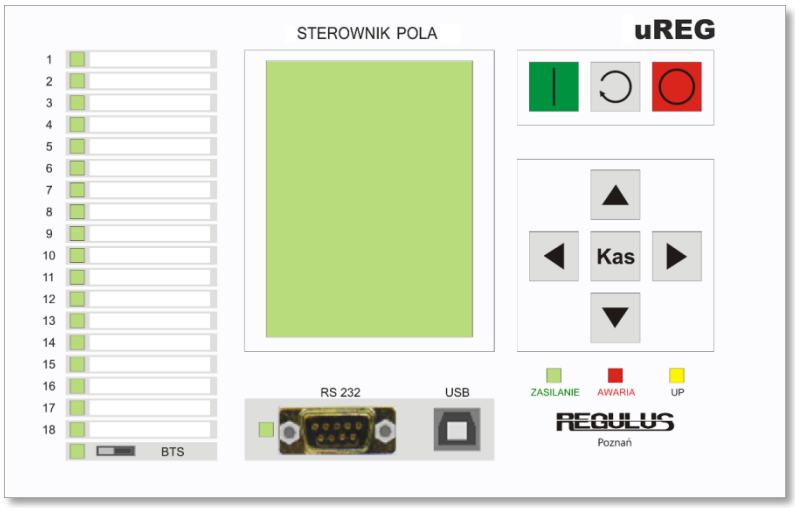


Fig. 8.1. View of the GH front panel.

- **GV** panel – graphic color LCD in TFT QVGA standard,
  in **vertical** arrangement;

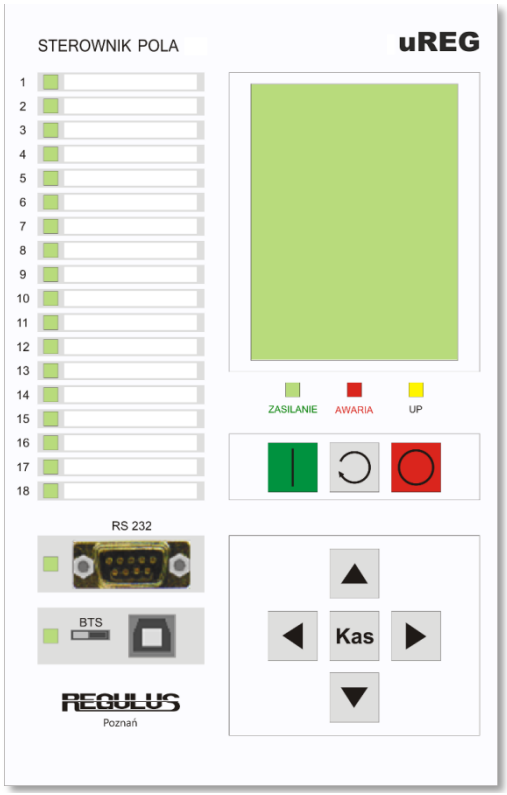


Fig. 8.2. View of the GV front panel.

- **NV** panel – with alphanumeric LCD,
  in **vertical** arrangement (corresponding to CZIP-1,2,3,4 protective unit panel).

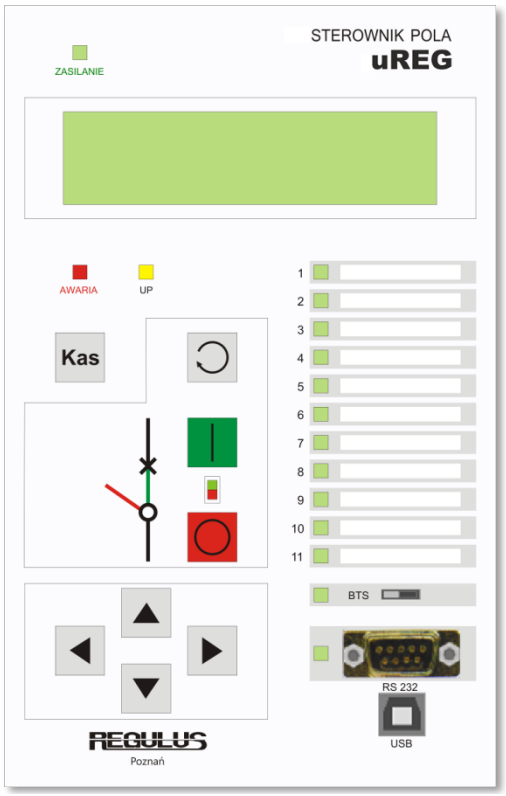


Fig. 8.3. View of the NV front panel.

The operator panel is connected to *uREG* using **one of 3 insulated** DB9F (female) connectors of the PN-485 interface (IF-0/IF-1 module), designated as **PANEL**.
The back wall of each panel has two identical DB9M (male) connectors to enable regular or 180-degree rotated installation.
Each panel can be connected to *uREG* as follows:

- integrally – from the front side (panel flush enclosure),
  from the back side (panel surface enclosure),
  or on the device side (lateral mounting);

or

- remotely - wired outside (e.g. to another room),
  over a distance up to 15 m.
  With this option, one of the DB9M ports on the panel back wall is provided with UNC thread barrels to be able to tighten the cable plug.

CAUTION:
The operator panel is an accessory, i.e. if there is no panel or it experiences a malfunction, operation of uREG *and its protective criteria to be executed will not be affected!*

Do NOT connect more than one panel to one* uREG *device!
Operation with 2 panels is available on special request only!

8.1. COMMON FEATURES OF THE PANELS

Common features of all *uREG* front panels:

- keyboard (8 buttons: ◄ ▲ ▼ ►, **Kas**, ON, **OFF**, **SEL**);
- buzzer;
- LEDs: POWER (green), FAILURE (red), UP (yellow);
- green LED informing about activity of communication interfaces (controlled by setting);
- RS-232 insulated communication link, type DB9M;
- USB communication port (type B);
- telecontrol interlock (BTS) switch with activity indication by a red LED;
- fields to describe LED signaling (using a soft marker or self-adhesive labels).

8.2. SIGNALING LEDs

All signaling LEDs (except BTS and interface activity signals) in *uREG* are **fully programmable**. Their activity strictly depends on the definition established in **APPLICATION**.

Standard LEDs, which are the same for all panel types, indicate:

- POWER (green) - testing working order of the unit;
- FAILURE (red) - failure-mode circuit-breaker tripping
- UP (yellow) - bay fault.
- The BTS **red** lamp lights up when the microswitch slider is moved to the ON position ← (left) and goes off when the slider is moved back to the OFF position → (right).
- The **green** lamp **signaling work of transmission interfaces** lights up to confirm that a correct message has been received via RS232/RS485/AUX RS485 serial links. Lighting status lasts for about 20 ms for each accepted and confirmed message. Signaling can be set independently by program for each of the listed interfaces by means of ***LED activity* setting**.

In addition, the panels are equipped with:

GH, GV **(graphic display)**	NV **(alphanumeric display)**
18 **red** LEDs	8 **red** / **green** LEDs
	3 **red** LEDs
	2 LEDs to visualize the circuit-breaker status:
	red – circuit-breaker opened,
	green – circuit-breaker closed.

CAUTION:

LEDs cannot be programmed via panel on the uREG *device.*
In order to define the response, the ***APPLICATION*** *layer must be accessed via* ***LogCZIP*** *. The procedure can have two outcomes:*

1. *LED association with a specific event (fixed association);*
2. *Definition of events having an effect on LEDs. The LED and its response to the event is selected by the user in* ***Monitor3****. The number of such events to be defined is unlimited.*

8.3. KEYBOARD

Meanings and functions of panel buttons result from the description implemented in the **APPLICATION**.

For typical cases and standard **APPLICATIONS**, the keyboard is used to navigate through screens and the protection menu, including the action of previewing and establishing settings. The keyboard has eight monostable buttons. Each time the button is pressed, a short audible signal follows (as defined in the **APPLICATION**).

- **Buttons** are marked with arrows: up (▲), down (▼), left (◄) and right (►). They strictly correspond to the structure and rules of access to usable information (menu) associated with the protection. Using the arrows, the user can navigate to each menu level and preview the information characteristic for a selected node or possibly initiate a corresponding action.
- The **Kas** button is used to confirm that the user has acknowledged important alarms on the LCD screen. Pressing this button may result in a wider range of effects if such features have been programmed.
- The **SEL** button is used to select by sequence mode of **ON** and **OFF** buttons (according to the current **APPLICATION**).
- The **ON** and **OFF** buttons are used to turn on/off the circuit-breaker and/or make/break bay disconnectors (according to the choice made previously using **SEL**). When pressed for the first time, the operation is prepared. Another pressing (after no longer than 2 s) means execution.

In *uREG* devices equipped with graphic LCD screens, pressing one of the buttons **ON**, **OFF** or **SEL** results in presentation of a mimic diagram (synoptic) and prepares the unit to change the circuit-breaker/disconnector state. The following text may be displayed:
`[* Control of switches]`, if defined accordingly in the **APPLICATION**.

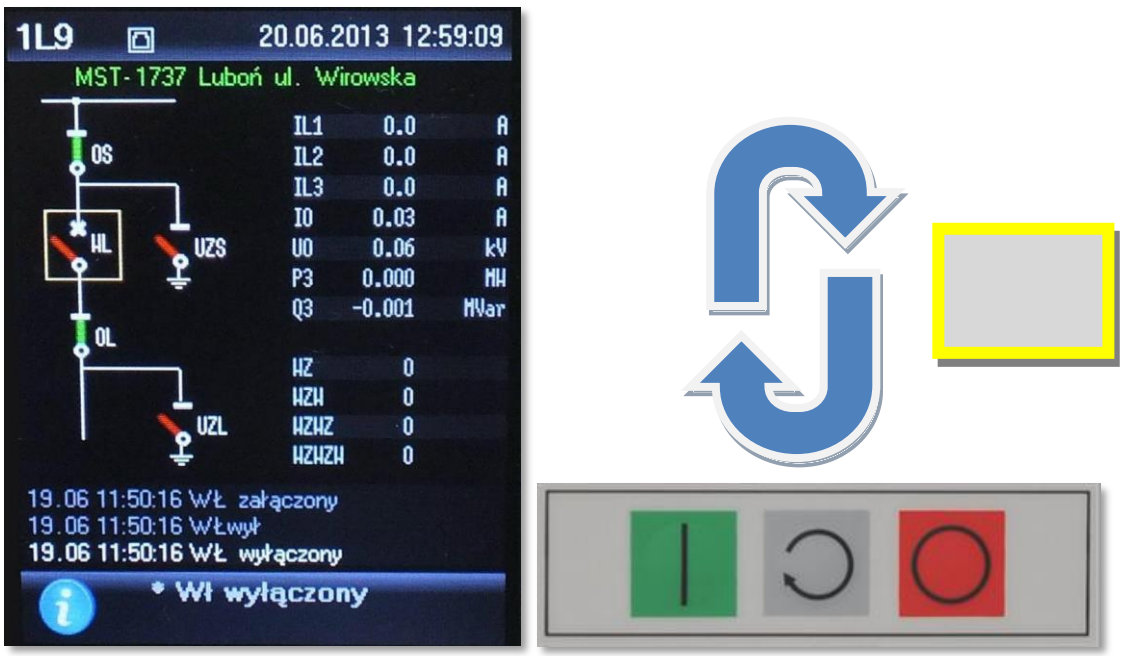


Fig. 8.4. Example of sequence-based selection of the circuit-breaker using **SEL** on the GH/GV panel display.

The selection is presented by the yellow frame displayed around the switch symbol. Pressing **SEL** changes cyclically the selection to the next circuit-breaker or disconnector. Shifting the selection to the bay disconnector is conditioned by unambiguous confirmation of the circuit-breaker tripping. After the programmed idle time for buttons **ON**, **OFF** or **SEL**, the application automatically changes the selection to the circuit-breaker (typically after 2 min.).

8.4. LCD SCREEN

8.4.1. MONOCHROMATIC ALPHANUMERIC DISPLAY

An alphanumeric LCD screen in the **NV** panel presents texts in two rows, 16 characters per row.

The display has a wide angle of view and high contrast as designed with STN standard The contrast value can be adjusted to fit the user's preferences and changing ambient temperature. Also, this is a LED-backlit display with adjustable light brightness. If the maximum temperature alert limit (65 ^{0}C) is exceeded, the display will be turned off in order to cool down.

8.4.2. COLOUR GRAPHIC DISPLAY

GH and **GV** operator panels are equipped with TFT graphic displays with the following parameters:

- diagonal 3.5 inch;
- resolution of 240 x 320 pixels (QVGA);
- 65 536 colors.

The contrast value can be adjusted to fit the user's preferences and changing ambient temperature. Also, there is a LED-backlit display with adjustable light brightness. If the maximum temperature alert limit (65 ^{0}C) is exceeded, the display will be turned off un order to cool down. Backlight of the TFT display is the main consumer of energy from the auxiliary power source. It is recommended to set a reasonable brightness level.

The display can show the following graphic and text items:

- application parameters, e.g. **1E6** where **1** denotes **hardware configuration** (→ section 7.15), the letter **E** identifies the application function, and the digit **6** is the version number/application release;
- current date and time (date format determined by settings);
- icons presenting UP status, data recorder status,
  active connections via ETH and USB interfaces, active re-indexation: UP ;
- programmable mimic diagram (synoptic);
- definable text, e.g. bay/substation name, etc.;
- measurements (definable sub-group);
- 3 most recent event reports;
- current message (→ text);
- menu with a characteristic icon (acc. to menu level).

In addition, a certain sub-group of screens, which create the so-called **Mini-Monitor**, is available to present:

- UP indications;
- event reports;
- primary measurements;
- secondary measurements;
- configuration of modules in the slots and states of digital inputs and outputs (from the side of module terminals) →

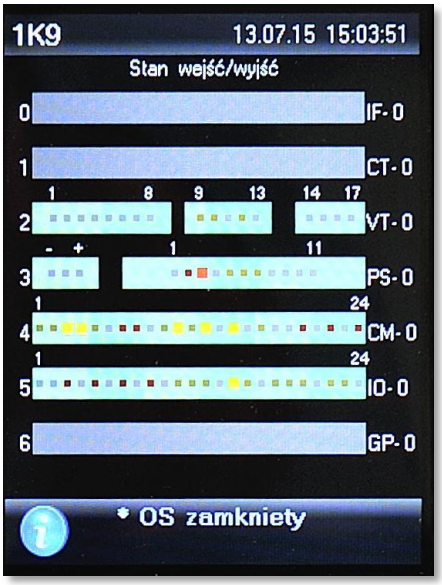


Fig. 8.5. Example screen presenting configuration of the module in slots and I/O states at module terminals.

8.4.3. TEXTS

Texts shown on the display are divided into types indicating the kind of the presented information. The texts are divided into:

- **notification** – all texts assigned to the information structure and alarm texts,
- **acknowledgement texts** – there are three levels of importance – low, moderate and high. The texts are presented on the display until **Kas** is pressed one time on the keyboard, or a text of higher importance is generated, or a remote TKAS erasure signal / TZ or ZW activation signal is received. New texts with a lower level of importance are withheld and queued during presentation of an important text. This type includes texts (with the sign !).
- **deleting texts** – used to delete acknowledgement texts, then presented as ordinary texts (e.g. text associated with the TKAS signal).

  Most texts are presented once. Texts presenting time-varying values as well as measurements or astronomical time are displayed in the auto refreshing mode. The refresh rate is approx. 2.5 images per second.

Apart from texts included in the information structure, the protection device can initiate on its own presentation of texts included in the numerous signaling and warning groups. This text type has no numerical identifier and, in the left corner, there is an exclamation mark (!) or asterisk (*) (or there is no specific leading mark at all). The explanation mark denotes a message describing an important event taking place inside the protection device, which is additionally commented in the report, and it usually requires an action to be taken by operating staff. Texts without leading marks document only the fact that a selected point in the algorithm has been accomplished.

*- For GH and GV graphic displays, additionally, one of the icons:  .

8.5. RS-232 COMMUNICATION LINK

The DB9M (male) insulated connector provides communication using serial information interchange with an external PC via EIA RS-232C interface. Transmission can be executed during normal functioning of the unit and is asynchronous at a programmable speed (300 Bd – 115 200 Bd) via *uCZIPstd* or *uCZIPnet* protocols.

Factory settings* of the RS-232 connector → 19 200 Bd, parity, full duplex, *uCZIPstd* protocol.
* – Conformity with default settings of CZIP and CZIP-1,2,3,4 units.

8.6. USB COMMUNICATION LINK (B-TYPE)

The Universal Serial Bus (USB) provides communication with an external PC (e.g. laptop/notebook) using a standard cable with A-type pins (from the PC side) and B-type pins (from the *u*REG side).
Transmission can be executed during normal functioning of the unit.

*u*REG is recognized by MS Windows (XP, Vista, 7, 8.1, 10 or higher) as HID (*Human Interface Device*) and requires no installation of any additional drivers on the system! The USB connector is also not associated with any setting in the *u*REG unit.

USB communication involves the *uCZIPstd* protocol.

Monitor3 is supplied together with the device. This program is used for quick, transparent and direct access to information in the *u*REG unit via RS-232 and/or USB. The program offers simple use of its functions (in particular, as regards setting programming), preview of events (reports), indications, measurements, counters, logger, etc.
The program maintains full and continuous communication with the protective device without any need for the user to perform manual adjustments.

9. *u*REG APPLICATION SOFTWARE

Brand new *u*REG controllers are provided by the manufacturer with complete control software (accordingly to requirements stated in the purchase order) so that the device can be quickly installed and put into service (→ **APPLICATION**).
If changes in your project assumptions occur or there are operational reasons, it is possible to replace the software in the base and application layers (→ section 6.2).
The latest firmware versions for basic bays in power system substations and typical industrial applications (e.g. wind power plants, hydroelectric power stations) are published by the manufacturer at http://www.regulus.poznan.pl.

In order to implement or reload the control software in all *u*REG controller reprogrammable components, the *u*REG utility program (supplied in a standard version together with the purchase pack or available on the manufacturer's website) must be used.

Regardless of standard applications for different purposes available on the Internet, it is possible to design and describe from scratch new customized applications or modify the existing ones. For these purposes, and in order to develop standard applications, REGULUS has devised a special solution:

Utility Software System
***Log*CZIP®**.

This comprehensive system is intended for the user to define formally the desired application, using simple, but still unambiguous, descriptions in a graphic form. The description elements are given as functional blocks (logic elements called **functors**) and their relations. The functors represent general multi-process computations, whereas relations between such elements refer to the sequence of events. The network, which is defined by means of functors and relations, presents the whole algorithm in a clear manner; the network describes itself and is comprehensive. There is a similarity to conventional logic networks with many features such as propagation time, hazard and deadlock. Although programming the application in *LogCZIP'* is not free from traps, it provides incomparably quicker programming than the conventional method, even is the application is complex and consists of many sheets.

*Log*CZIP consists of many components. The most important ones include:

- application project management system,
- MDI graphic editor for application sheets,
- interpretation-based syntax analyzer,
- project compiler,
- static debugger,
- dynamic debugger,
- configuration file generator to be used with *Monitor3*,
- programmer.

9.1. EDITING THE *Log*CZIP APPLICATION

Any application (project) is described using one or many program sheet(s). The number of sheets to be used is unlimited and has no logic meaning. Dividing the project into sheets (and their corresponding number) is associated with maintaining project readability, not formal requirements. Also, the developer's individual style of programming is important.
The sheets are given distinct names to make them distinguishable. Information relations between the sheets (signals) are described (declared) using **labels**.

The basic component of an application description is given by **a functor**,
which represents conditional computation and, in the simplest case, consists of two items:
- relevant functional block,

and
- logic gate to set the condition for functional block activation.

The binary computation state of the functional block is reproduced at the functor output to reveal it to related **following-type** functors. The logic gate monitors binary states of **preceding-type** functors associated with the gate. The binary high state on the functor output is called 'activation state'.

Complex functors usually have a few logic outputs, but no more than eight. In this case, the activation state of the logic output results from the state of partial computation relating to the functor associated with the output. The outputs are numbered from zero to the maximum number. For functors with a lower than eight number of logic outputs, the output states are reproduced on several physical outputs (not visible graphically), in uniform groups, until the group of eight outputs is used up.
The number of outputs is usually a multiple value of the base 2, hence: 1, 2, 4 or 8.

Similarly for many outputs, functors can generally have more than one conditioning gate on the input. Then input gates set various partial conditions to initiate computation in the functional block. The total number of inputs of all gates is always eight. The inputs are numbered from zero to seven. Therefore, the gates share the input pool in logically uniform groups with 1, 2, 4 or 8 inputs.

The number of logic outputs and conditional gates determine connecting capability of the functor. As the number of outputs and gates increases, this capacity is reduced. The situation results from optimization purposes since the possibility of relating the functor input with a given number to a physical output with the same number in the preceding-type functor, which serves for the signal source. The connecting capability can be fully restored if simple intermediate functors (gates) are applied.

An example functor with two outputs and two gates on the input is shown in the following figure. The top gate computes the logic sum of inputs 0 to 3, whereas the bottom gate, the conjunction of states from inputs 4 to 7. The logic state 0 on the output is reproduced on physical outputs 0 to 3 (not shown in the drawing), whereas the output state 1 is reproduced on physical outputs 4 to 7.

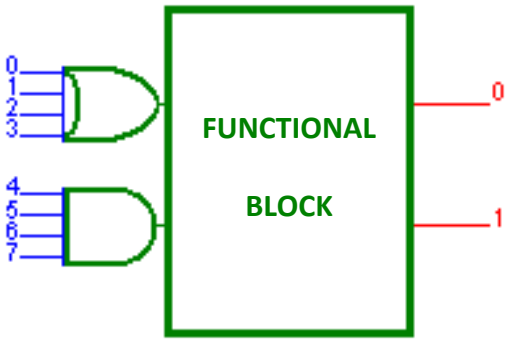


Fig. 9.1. Example functor

Some functors are equipped with one or more variable parameter(s) to modify computation in the functional block. These parameters given as **settings** are accessible in the utility software – *Monitor3*; the values can be changed as the application is evaluated.
While developing the application, the developer determines some features of settings (e.g. precision of counting time delays), assigns names to chosen settings (if other names than default ones are required), assigns settings to one of the defined **setting groups**, assigns names to chosen setting values and decides on conditions of access to the setting.

Each functor output is assigned with an initial **DNP-3.0 protocol index**. The output index with the number 0 can be arbitrarily (but not in contradiction to other indices) defined and modified at the stage of application description. Indices of subsequent functor outputs are consecutive values of the output index 0. The functor in the figure takes two indices with the number n for the output 0 and the number n+1 for the output 1.

For each functor output (and thus, for each DNP-3.0 index), capability for generating a **report** about each or a specified change in the logic state can be assigned. The report can be described with a text as desired. Selected reports can be assigned to **class 1** in DNP-3.0 or independently classified for presentation on the *Monitor3* screen or be included to a set of events presented in the window of **UP** *bay fault indication*.

Output activation can also result in generation of **a text** presented on the device display and the *Monitor3* screen. The text information is determined in the course of application development. The text can have up to 32 characters.

Functors are inserted into the program sheet by loading them from the collection set available in the *LogCZIP* editor. Functors representing virtual resources (like logic gates, analogue inputs, etc.) can be inserted into sheets in any number, whereas other elements associated with physical resources (like inputs from terminals, relays, etc.) can be inserted until their number is the collection set is used up.
Once necessary functors are arranged in the sheet, they must be related to **lines** or **labeled lines**. The line drawing mode is activated by the pencil icon */Edycja → Rysuj/*. Labels are equivalent to the line to which they are attached. (These are an abstract extension of the line to be able to transfer links to other project sheets.). The label also assigns the relation name. Lines without labels are unnamed.

The relation must meet correctness conditions. Some of them are verified on an ongoing basis in the graphic editor, whereas other conditions, during project compilation. Improper or impossible relations must be corrected until correctness is confirmed. This process may require selection of other functors or addition of intermediate functors to improve connecting capability.

Readability of the application project can be essentially improved by adding texts (→ **comments**). Comments do not have any logic meaning; they can be added in any place in the sheet and in any order. They usually supplement the information provided by label names of relations and functors.

List of **basic** functors divided onto classes.

➢ Functors of **logic gates** [7]:

- OR gate
- AND gate
- NOR gate
- NAND gate
- XOR gate
- XNOR gate
- 2AND-OR gate

➢ **System-related** functors [65], such as:

- system reports /obligatory/
- internal corrections
- alarm
- indexation of primary measurements
- extended indexation of primary meas.
- extended indexation of secondary meas.
- extended indexation of external meas.
- external parameters S1, S2, S3
- time zones
- limit currents
- computer links
- LCD display
- LCD blanking
- LCD automatic unit
- event deleting
- power unit efficiency
- protocol IEC 60870-5-103
- protocol IEC 60870-5-103 – interference no.
- keyboard buttons
- data recorder
- date format on LCD
- protocols IEC 60870-5-101,60870-5-104
- spontaneous DNP3
- selection of measurements for LCD and Monitor3
- ATS line selector
- keyboard limiter and password
- measurements of section 1a / 1b [MSK]
- measurements of section 1a / 1b [MSK]
- measurement of section 1 [MSK]
- measurement of section 2 [MSK]
- selection of switch 01 ÷ 13
- BKR clock
- ATS line selector
- strobe generator
- CZIPstd protocol
- MODBUS protocol
- CAN PPM2 protocol
- SCADA DNP3
- criteria recorder
- functors for selection of ON/OFF operations for the mimic system (different types)

➢ **Functors of standalone settings [7]:**

- 1-bit setting
- 2-bit setting
- 4-bit setting
- 8-bit setting
- settings bank change
- setting redefinition
- computer-based change in settings bank

➢ Functors of **analogue inputs** [acc. to configuration of modules], in particular:

- overcurrent criterion I>
- tripped overcurrent criterion I>T
- overcurrent criterion I0>
- differential fault protection dI>
- current criterion of computed zero sequence L0>
- current asymmetry criterion aI>
- undervoltage criterion U< AND and OR
- tripped undervoltage criterion U<T
- overvoltage criterion U> AND and OR
- tripped overvoltage criterion U>T
- over and underfrequency criterion f><
- derivative frequency criterion (df/dt)>
- second harmonic criterion f100>
- SPZ/SCO internal criterion
- overvoltage criterion U0>
- admittance criterion Y0>
- conductance criterion G0>
- conductance directional criterion G0k>
- susceptance directional criterion B0k>
- comparative-admittance criterion YY0>
- reactive underpower criterion Q3f<
- reactive overpower criterion Q3f>
- active overpower criterion P3f>
- active underpower criterion P3f<
- directional power interlock AND and OR
- capacitor bank /BKR/ controller
- AWSCz controller
- voltage derivative criterion dU/dt<
- voltage derivative criterion dU/dt<
- synchro-check [VT-2]
- difference of sectional voltages dU<
- difference of sectional voltages dU>
- deltaf< [in Section 1-2]
- U1>, U2>, U3> for MSK
- I1>, I2>, I3> for MSK
- Vector Shift

➢ Functors **of signal crossovers** [8]:

- AND ISNT (ie. and IS not yes)
- AND ISTN (ie. and IS yes not)
- AND SINT
- AND SITN
- OR ISNT
- OR ISTN
- OR SINT
- OR SITN

➢ **Flip-flops** [17]:

- monoflop AND_P N
- monoflop OR_P N
- OR_N 1 monoflop
- level-controlled RS flip-flop
- monoflop AND_PN 1
- monoflop OR_P 1

- level-controlled RS flip-flop (non-volatile)
- level-controlled SR flip-flop
- Q-edge controlled RS flip-flop
- Q-edge controlled SR flip-flop
- QQ*-edge controlled SR flip-flop
- Edge-controlled D flip-flop
- Edge-controlled D flip-flop with reset
- volatile SR flip-flop, released by positive edge with Q OR-AND output
- volatile SR flip-flop, released by positive edge with Q AND-OR output
- volatile RS flip-flop, released by positive edge with Q OR-AND output
- volatile RS flip-flop, released by positive edge with Q AND-OR output

➢ **Time delays and pulse formation** [15]:

- pulse generator
- pulse extender circuit type 0 no restart
- pulse extender circuit type 1 with restart
- pulse extender circuit type 2 with input logic sum
- pulse extender circuit type 3 no restart
- positive pulse delay type 4 OR
- positive pulse delay type 5 AND
- double-edge delay type 6
- pulse release type 7 no restart with reset
- pulse delay type 8 activated by negative edge
- pulse release type 10 no restart AND
- pulse delay type 11 XOR
- N-cycle delay 1
- N-cycle delay 2
- delay type 12

➢ **Counters** [6]:

- 2-bit counter with decoder
- sequencer with conditions
- SPZ cycle counter
- 3-bit counter with decoder
- SZR /ATS/ cycle counter
- ZS cycle counter

➢ **Decoders** [6]:

- 1-of-4 decoder
- 1-of-4 decoder (conditional)
- 1-of-8 decoder
- demultiplexer (3 in 8)
- 1-of-8 decoder (inverted)
- 1-of-8 decoder (with prohibition input)

➢ **Markers** [4]:

- AND Report & Exit (defined be setting)
- NAND Report & Exit (defined be setting)
- NOR Report & Exit (defined be setting)
- OR Report & Exit (defined be setting)

➢ Functors of **mimic boards** /synoptics/ [10]:

- SZR /ATS/ interlock No
- SZR /ATS/ ready No
- SZR /ATS/ interlock Yes
- SZR /ATS/ ready Yes

- Automatic control No
- BREAKER open
- ON active
- Automatic control Yes
- BREAKER closed
- ON inactive

➢ Functors of audible alarms [1]:
- Buzzer

➢ Functors of **digital inputs** [acc. to configuration of modules]:
- BTS switch
- ▼ button
- ▲ button
- ◄ button
- ► button
- SEL button
- KAS button
- ON button
- OFF button
- power contact control
- /protocol/ computer input
- AC 24/220 bipolar input with setting
- DC unipolar input
- DC unipolar input with adjustable sensitivity threshold

➢ Functors of **relays** [acc. to configuration of modules]:
- AL relay
- power relay
- switchable relay
- make-contact relay OR
- make-contact relay AND
- /protocol/ computer output

➢ Functors of **LEDs** [acc. to panel configuration]:
- LED Power – green
- LED Failure – red
- LED UP – yellow
- Red LED
- Green LED
- LED – definable /event/

9.2. PROJECT COMPILATION

Once edited using the graphic editor, the application project has to be compiled. The compilation process is called from the toolbar in the editor by clicking the gear icon /*Narzędzia → Kompilacja projektu*/. Compilation includes a syntactic analysis of the project to check its correctness and feasibility of relations between functors. The project whose syntax is correct undergoes optimization. This process may or may not result in renaming identifiers (numbers) relating to functors.

Compilation of a correct application project yields:

- output HEX files with the application code for direct upload to the controller (also *.APP packed file for external uPROG programmer),
- output files with the settings code for direct upload to the controller,
- application signature which unambiguously identifies the application,
- output CFG files generated for *Monitor3* so that the program can be used to handle the application,
- compilation status providing information about the number of applied functors, settings, reports, texts and the project signature.

The output files with the code and settings can be immediately reloaded to the controller (in on-line mode if the device is interfaced with the editing computer), or later with the use of a external uPROG programmer. For the immediate mode, the programmer is called by clicking the integrated circuit upload icon /*Narzędzia → Programowanie uREG*/.

9.3. STATIC DEBUGGER

Successfully completed compilation automatically activates the environment for a local or remote **static debugger** of the project. Irrespectively of the access mode, the debugger is called by the black triangle icon on the tool bar in the editor /*Debugger → Krok elementarny*/.

The debugger is used to test and monitor complete operation of the finished application project under conditions which will be identical for controller computers (except the real-time conditions). Thus, application evaluation and tracking computation progress is performed in a model electrical environment in virtual time, with steps simulating the lapse of elementary time units or their conventionally agreed multiple values.

Emulation of an actual electrical environment in the switchboard uses a dedicated analogue input window in the *LogCZIP* system. Rows in the window can be used to impose at any moment the desired substitute values of currents, voltages, phase current phases relative to voltages and zero sequence phase relative to voltage and frequency and its derivative. For debugging double-section equipment (like ATS), voltages across busbars can be set independently for each section.

Logic levels of substitute digital signals across device terminals and computer signals are determined in windows presenting attributes of functors associated with relevant inputs. Such

states can be imposed completely asynchronously relative to the application evaluation process.

The state of evaluation and computation progress is visualized on the PC monitor in dedicated windows and the project sheet. The most important aspect here is to ensure direct representation (in program sheets) of activation states on functor outputs using square markers drawn on the output lines. The activation state is represented by a red-filled rectangle, whereas the passive state, by a red-contour white-filled rectangle. States on functor outputs are reproduced for all inputs associated with the output using similar dark blue rectangles, while the same logic is maintained: activated input – color background, inactive input – white background. This information, which is fundamental for recognition of the logic state of individual functors and the entire application, is completed with additional components describing the process state of some functors, in particular time-delay functors. For the last case, states of timers can be monitored in the sheet in the vicinity of functors. If the remaining time delays(s) is (are) known, the evaluation process can be accelerated by emulation of virtual time at steps which are multiple values of the elementary unit, e.g. 1-second units.

Evaluation progress and results are complementarily presented in many specific windows in *Log*CZIP debugger. These include, in particular:

- debugger log window (with records relating to all actions on functors (with identifiers of such elements specified), input and output states, number of state transitions, reports and texts generated by functors, changes of analogue inputs and emulation of digital inputs – the window also presents the virtual clock state and the number of applied elementary units;
- event report window with events generated by functors (the structure is similar to the one in *Monitor3*);
- LCD screen window presenting current and upcoming texts sent from functors to the display;
- functor evaluation window presenting identifiers of functors which completed evaluation and elements with pending evaluation.

9.4. *u*REG DYNAMIC DEBUGGER

The **dynamic debugger** is used to monitor the current state of the application under any condition. This sub-system is a component of the *Log*CZIP utility software, called from the tab */Debugger → Debugger Online/*.

The debugger operates in on-line mode together with an **active** *u*REG controller via computer link and visualizes states of functors on the PC monitor (in application sheets). State visualization means reproduction of the principle used in the static debugger, i.e. activation states are shown by red-filled rectangles for outputs, dark blue rectangles for inputs, white-filled rectangles for inactive states of inputs and outputs.

The dynamic debugger is a very useful tool in two cases:

- during checks and tests of correct operation of a new or modified application (for this purpose, the debugger can be used as an independent tester or as an essential final addition to tests performed using the static debugger);
- during installation and maintenance of the device to confirm compatibility with the bay design, and during routine operation to resolve doubts associated with the algorithm as well as past control and activation operations.

10. *u*REG START-UP

In order to start the device, apply auxiliary voltage as specified to the terminals [**+**] and [**-**] and install an earthing conductor at the terminal [⏚]:
auxiliary voltage sources:

- 88 to 350 V DC / 230 V AC for the **PS-0** module, or
- 21 to 38 V DC for the **PS-1** module

(in slot #3 and/or #6 or on both slots). Then *uREG* will start up. For color graphic display panels (**GH**, **GV**), the following test image (example) will be displayed for a while:

Fig. 10.1. Test pattern on the display

The panel equipped with a **NV** alphanumeric display will show:

```
* uREG panel *
REGULUS – Poznań
```

10.1. BOOT mode

Depending on other programmed software layers for the main computer, the LCD screen will show one of the following texts:

BOOT modes

```
*   uREG Boot
(C)  REGULUS
```

or

```
*  uREG Boot XXX
REGULUS [ info ]
```

- where the optional field **XXX** can assume the following values: **POR, 4BT, RET**

which should be understood as follows:

- **POR** /**P**ower **O**n **R**eset/ – *u*REG has been reset by auxiliary power-off;
- **4BT** /**4 Bu**ttons Reset/ – the user has intentionally set *u*REG in **BOOT** mode (by pressing and holding all 4 arrow buttons during auxiliary power-up). This is also known as *emergency/service mode*.
- **RET** /Application **Ret**urn/ – *u*REG has returned to **BOOT** mode, e.g. during initialization of programming of another application;

- where the optional field **`[ info ]`** can assume the following values: **`NoBase, No App, FlaErr, AppOK,`**

which should be understood as follows:

- **[NoBase]** – device in **BOOT** mode, no lower layer (**BASE**) is programmed (see → *u*REG **BASE**). This is also known as *factory mode*.
- **[No App]** – missing application → *u*REG in **BOOT** mode, **BASE** is programmed, but no functional **APPLICATION** has been programmed. This is also known as *factory mode*. It can also occur after the user exchanges / updates **BASE**.
- **[FlaErr]** – Flash memory error → *u*REG in **BOOT** mode, **BASE** and functional **APPLICATION** are improperly programmed and cannot be started and/or a flash memory sector is damaged/corrupted.
- **[App OK]** – *u*REG in **BOOT** mode, **BASE** and functional **APPLICATION** are properly programmed, but the user has **intentionally** switched the device to *BOOT* mode, e.g. *for service purposes*.

In **BOOT** mode, pressing any buttons on the panel will display the *u*REG serial number.

CAUTION:

- *If the device has a programmed **APPLICATION**, the device will start up in **APPLICATION** mode.*
- *Forcing **BOOT** mode is always possible by pressing and holding all 4 arrow buttons on the operator panel during auxiliary power-up on uREG !*
- *In **BOOT** mode, it is possible for uREG to operate together with the* Monitor3 *program to modify auxiliary settings (relating to transmission and LCD).*
- *In **BOOT** mode, a test pattern will be continuously displayed on **GH** and **GV** panels.*

10.2. APPLICATION mode

10.2.1. START AND VERIFICATION

*u*REG performs tasks associated with system initialization, including configuration verification, self-tests and calibration of measurement paths. Although these tasks are performed quickly, hey are still visible on the LCD.

CAUTION:
*uREG will be **ready for operation** provided that verification of hardware configuration (compatibility of modules in slots with **the application project**) is successful and **suitable for the currently active APPLICATION** or **more advanced in terms of the project**.*
Then the alphanumeric display will show the last valid text as generated, whereas the graphic display will show the last valid generated text together with a bay mimic diagram (main screen).

In case of **hardware configuration incompatibility** with the application project (insufficient number of modules and/or improper allocation of slots), the display will show the text:

```
! Brak zgodności
 sprzętu z apl.
```

For the graphic display, up to 4 missing/misconfigured modules will be additionally listed, e.g.:

```
Slot 1: brak dostępu do płyty CT-0 /no access to CT-0 board/
Slot 2: brak dostępu do płyty VT-0 /no access to VT-0 board/
```

and the warning icon displayed:

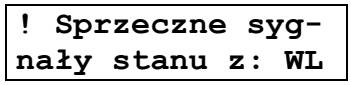
Fig. 10.2. Indication of hardware incompatibility with the application (graphic panels)

CAUTION:
*Once hardware configuration incompatibility is found, the device will lock all protective functions and handle **only communications ports** while waiting for **hardware reconfiguration** or **programming another application** (dedicated to the current module arrangement)!*

10.2.2. OPERATION

Specific behavior of the device depends on the state of external digital and analogue signals and the mode to handle them as defined in **APPLICATION**.

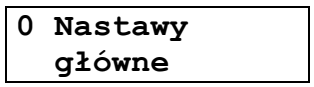
For applications supplied by REGULUS, in case inconsistent digital logic states on one of the switches or the circuit-breaker are identified, a relevant text will be displayed on the LCD screen. This may be a piece of information as follows:



⇨ **Inconsistent state signals from breaker**

If the described condition occurs, the device will also give an intermittent audible alarm on faulty external circuits. The alarmed state is cancelled by pressing **Kas**. Acknowledgment of all improper states turns off audible alarms, and the display shows the last message generated by the device.

By pressing ◄ (left) or ► (right) , the following screen will be displayed:



⇨ **Main settings**

This screen is the level to start navigation through → **menu** of *u*REG.

For **GH** and **GV** panels, press ▲ (up) to go to the so-called **Mini-Monitor** and display its first screen, i.e. bay fault indication.
Press ▼ (down) to go to the measurement screen (increased font size).

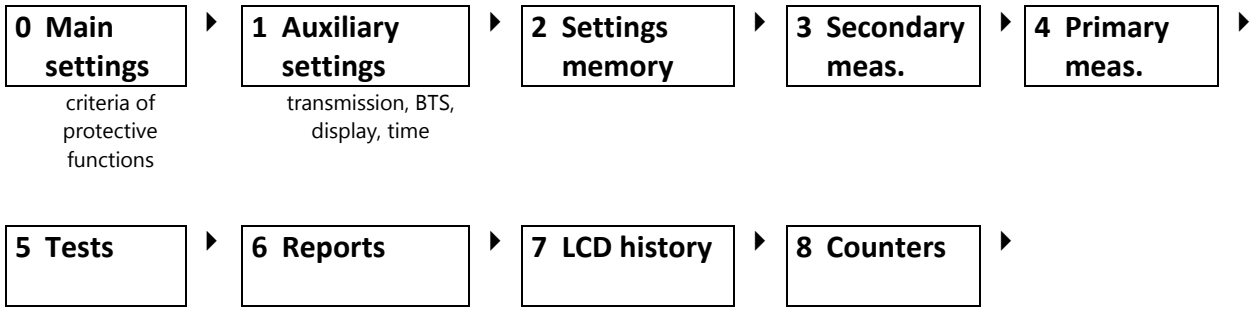
Pressing **Kas** will always resume presentation of the synoptic mimic diagram (main screen).

11. MENU

*u*REG allows the user to make decisions on several useful information, which create the so-called **menu**.
The structure and navigation through menu is similar to those in CZIP i CZIP-1,2,3,4 – menu resembles a structure of an inverted tree.

Each screen in the structure has a numerical identifier (**IDENT**, upper left corner), wherein **the number of digits corresponds to the ident level**. **Once the protective device is turned on or restarted, pressing the left arrow button ◄ or right arrow button ► starts the initial-level menu (identifier 0).**
The first level includes nine main nodes (from 0 to 8).
*u*REG with a GH/GV graphic display also has an additional 10th node (marked as 9) for **Status of digital inputs/outputs**.

Main groups of the structure are shown on the LCD screen as the following screens:



+ optionally (for **GH** and **GV** graphic displays):

By pressing the button once, the user is navigated to the closest node in a respective direction. The presented example shows how to toggle main groups (**navigate from node 0 to node 8** [or 9]) **by pressing ►**.

For the left and right directions, if the nodes have many adjacent sub-groups, there is a clock-like mechanism to speed up the preview experience. The mechanism activates automatically once the button is pressed and held for a while. Navigating through the structure means moving from one end-node to another (without automatic scrolling).

Buttons ▲ and ▼ are used to navigate the user to the function available one level up or down (depending on the direction). For example, for menu **0 Main settings** or **1 Auxiliary settings**, the navigation process ends by presenting the setting value.

Further, changing a setting value requires pressing ◄ (previous value) or ► (next value). With graphic displays, changing the active value of the setting is additionally signaled by changing the color to orange.

For the *u*REG device equipped with a graphic display, pressing **Kas** shifts to presentation the mimic diagram (main screen).
Operating *u*REG is much easier if external software is used (→ see *Monitor3*), which can run on OS Windows (recommended XP, 7 or higher).

A description of *u*REG with numerical identifiers, which are particularly useful for keyboard operations, and basic information about working with *Monitor3*, is provided in Table 11.1.

Table 11.1.

IDENT	MENU description	Button in Monitor3 / Comments
0	**Main settings**	**F10**
00	Setting group 0 (subject-related, depending on the application)	
000	Setting 0 in group 0	
0000	Value of setting 0 in group 0	
…		
00n	Setting n in group 0	
00n0	Value of setting n in group 0	
…		
…		
0n	Setting group n (subject-related, depending on the application)	
0nn	Setting n in group n	
0nn0	Value of setting n in group n	
1	**Auxiliary settings**	**F9**
10	LCD display	
100	Brightness	*The effect of a changed setting is shown on the display.*
1000	Value of brightness setting	
101	Contrast	
1010	Value of contrast setting	
11	UART communication	
11n	UARTn setting	
11n0	UARTn setting value	
12	Ethernet communication	
12n	ETHn setting	
12n0	ETHn setting value	
13	Astronomical time	**Ctrl+F10**

130	Current time	
1300	yy:mm:dd:hh:mm:ss	
131	Changing time: correct year	
1310	Correct year rr	
132	Changing time: correct month	
1320	Month mm	
133	Changing time: correct day	
1330	Day dd	
134	Changing time: correct hour	
1340	Hour hh	
135	Changing time: correct minutes	
1350	Minutes mm	
136	Changing time clock	**Setting available only via panel keyboard**
1360	Inactive/active correction	
2	**Settings memory**	**F2**
20	Restore settings of functors	
21	Password I for functors settings	**No password is required in Monitor3 to change settings**
22	Password II for functors settings	
23	Fix main settings	
24	Restore TRX* and LCD settings	**TRX → transmission*
25	Password I for TRX and LCD settings	**No password is required in Monitor3 to change settings**
26	Password II for TRX and LCD settings	
27	Fix auxiliary TRX and LCD settings	
3	**Secondary measurements**	**F7**
30	Current IL1	
31	Current IL2	
32	Current IL3	
33	Current Ifmax	
34	Current I0	
35	Current Ig	
37	…..	*Continued list → see Secondary measurements*
4	**Primary measurements**	**F7, F6 (power and energy measurements in time zones)**
40	Current IL1	
41	Current IL2	
42	Current IL3	
43	Current Ifmax	

44	Current I0	
45	Current Ig	
47	…..	*Continued list → see Primary measurements*
5	**Tests**	**F4**
50	Internal measurements	**Ctrl + I**
500..509	Measurements of system parameters	*Continued list → see Internal measurements*
51	LED test	
510	Activate LED test	
52	Serial number	*Serial number and uREG version*
520	Number **N**rr nnn**u**bbapm	
53	Project signature	*Active uREG application signature*
530	Signature **sssssssssssssss**	
6	**Reports**	**F5**
60	Event reports	*Event reports presented in yellow (GV, GH)*
	Event report	
7	**LCD history**	**F3**
70	LCD history	*Historical texts presented in green (GV, GH) or on dimmed display (NV)*
	Historical text	
8	**Counters**	**Shift+F8**
80	OFF number for range 1: I	
81	OFF number for range 2: I	
82	OFF number for range 3: I	
83	OFF number for range 4: I	
84	Number of cycles: SPZ wz c	
85	Number of cycles: SPZ wzw c	
86	Number of cycles: SPZ wzwz c	
87	Number of cycles: SPZ wzwzw c	
88	Number of cycles: SPZ wzwzwz c	
89	Number of cycles: SPZ wzwzwzw c	
9	**Digital inputs/outputs**	**F8, Ctrl+F8**
90	I/O state for graphic LCD	

12. KEYBOARD OPERATIONS

This chapter should familiarize the user with the rules relating to keyboard operations based on examples with the password required to access settings, how to set astronomical time and change display settings.

12.1. PASSWORD

Security rules require that access to most settings should be protected with a 2-level password.

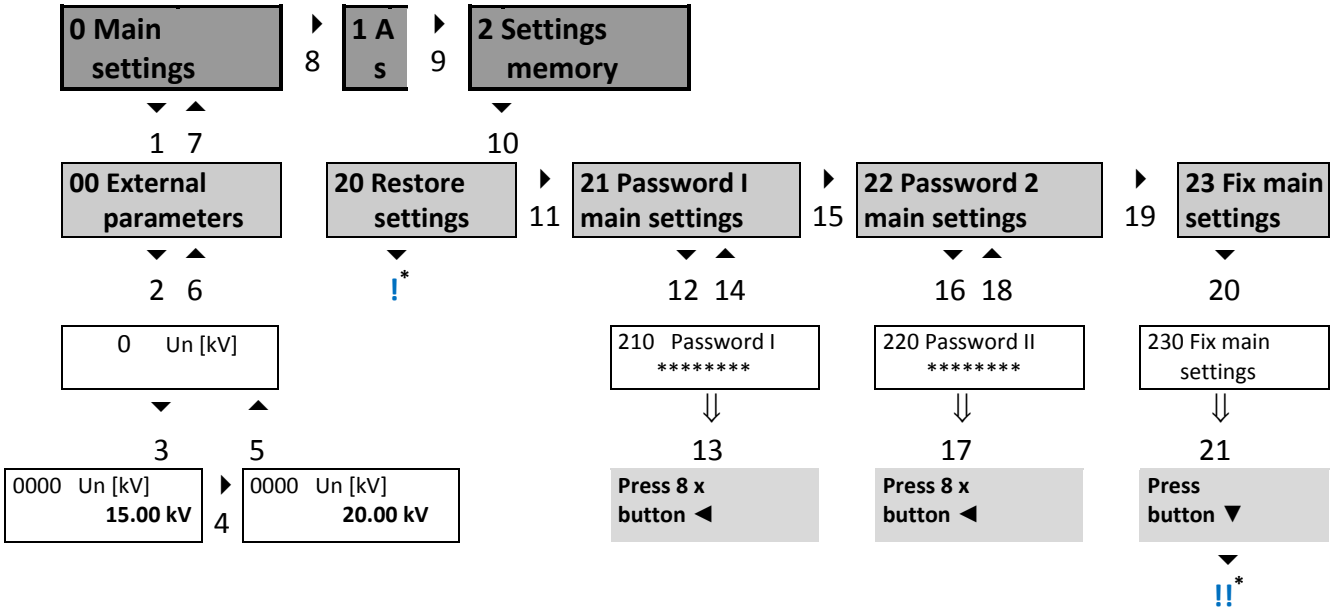
CAUTION:
The password assigned by the manufacturer involves pressing ◄ 8 times (consecutively). The same password is used for access to level I and level II.

The password is required for:

- redefinition of functors settings — 69→ ident 0 **Main settings**;
- redefinition of auxiliary settings — 69→ ident 1 **Auxiliary settings.**

A new password should be assigned by using *Monitor3*.
Please refer to *Monitor3* to restore your forgotten password.

The following examples present changes in settings secured by a password. The example shows how to navigate through menu to change the setting of rated primary voltage UN from 15 kV to 20 kV. Starting point → group **0 Main settings**.

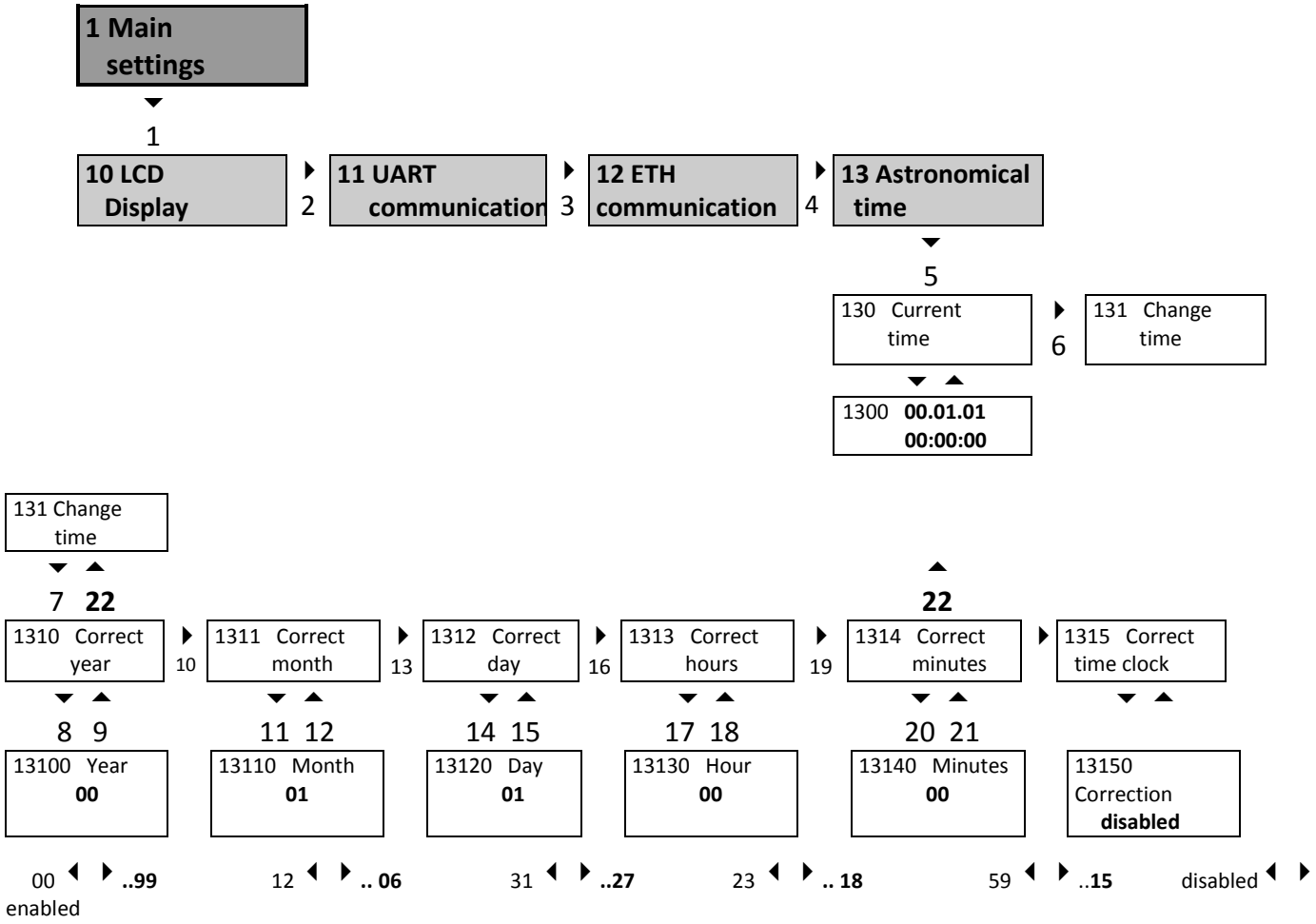


*! *! – Wait until "! Settings restored" appears. **This option means cancellation of new settings.** The display will show values restored from the device memory. It is recommended to restore settings routinely when settings are read out on the display to eliminate effectively accidental changes in settings (not confirmed by the password), which provides a true picture of the information saved in the settings memory.
This operation is equivalent to a repeated readout using *Monitor3*.

*!! *! – Wait until "! Settings fixed" or "! Fixed setting discarded" appears (if the password is incorrect).

12.2. DATE AND TIME SETTINGS

Changing time settings requires auxiliary voltage power-up. This example shows how to change date from **2000.01.01** to **2011.06.27**, and time from **00.00.00** to **18.15.00**.



Changing time settings is performed in step #22 by navigating to the '**131 Change time**' screen. Then the seconds counter is reset, and as such the clock can be synchronized with an accuracy of 1 second.

Accuracy correction (see screen '**1315 Correct time clock**') is set by the manufacturer. The user shall refrain from any changes.

While working with *Monitor3*, changing time settings can be automatic based on the time clock of the internal computer.

12.3. DISPLAY SETTINGS

Display parameters are accessible in the sub-group '**10 LCD screen**' where auxiliary settings are provided. They are associated with the LCD screen to adapt it to the user's preferences. The group '**7 LCD history**' provides previewing previous texts.

12.3.1. BRIGHTNESS & CONTRAST

Brightness (ident 100) – used to set display backlight intensity using LEDs. Once saved, the setting is the default value obeyed by the device until it is restarted or settings are restored. In addition, any brightness change is applied immediately to present the user with the effect.

Contrast (ident 101) – used to set dot blacking on the LCD screen. Image contrast is a function of temperature and requires correction upon major ambient temperature changes. Once saved, the setting is the default contrast value obeyed by the device until it is restarted or settings are restored. In addition, any contrast change is applied immediately to present the user with the effect.

CAUTION:
The user is advised against saving a contrast setting with complete image disappearance, as no message can be read and restoration of the correct state is more difficult. If this is the case, it is recommended to use a computer and Monitor3.

12.3.2. HISTORY

In order to facilitate previewing texts, in particular if the rate of new texts is high, the information structure is provided with an additional group marked as Ident '**7 LCD history**' which provides access to previous texts (generated earlier) in their sequence of occurrence on the display (without any time restraints). **The bottom level to go back into previous texts is 64** from the level when entering '**LCD history**'. Every time a new preview of historical texts is initiated, the latest text relative to the present moment is displayed.

Entering the history level is confirmed by:

- **reduced brightness** (for the **NV** alphanumeric display)

or

- **texts displayed in light green** (for **GH** and **GV** graphic displays).

Previewing historical texts does not prevent the display from presenting current texts.

12.4. MINI-MONITOR (GH / GV)

GH and **GV** panels with color graphic displays provide additional information screens, the so-called **Mini-Monitor**, activated by pressing ▲ (up) when the main screen is displayed. → See **Mimic diagram (Synoptic)**.
Press ◄ ► to toggle screens and ▲ ▼ to scroll screens.
Press **Kas** to resume presentation of the mimic diagram (main screen).

13. MEASUREMENTS

The *u*REG unit has been designed for two purposes: the primary aim to provide protective functions and, additionally, to take electrical measurements during operation of a substation bay.

Provision of both objectives requires regular basic measurements of bay electrical parameters. The *u*REG unit measures 12 essential analogue value, the base for provision of protective criteria. Depending on hardware configurations, these measurement can be as follows:

- three phase currents: IL1, IL2, IL3 (from module **CT-0**);
- three line-to-line voltages: UL12, UL23, UL31 (from module **VT-0**);
- two currents: zero sequence I0 and Ig (from module **VT-0**);
- zero sequence voltage U0 (from module **VT-0**);
- three voltages at inputs AUXI0, AUXI1, AUXI2 (from module **VT-0**)

or

- three phase currents: IL1, IL2, IL3 (from module **CT-0 and VT-3**);
- three line-to-line voltages in section 1: UL12, UL23, UL31 (from module **VT-2 and VT-3**);
- three line-to-line voltages in section 2: UL12, UL23, UL31 (from module **VT-2 and VT-3**);
- zero sequence voltage U0 in section 1 (from module **VT-2**);
- zero sequence voltage U0 in section 2 (from module **VT-2**);
- zero sequence current I0 (from module **VT-2**);

The listed values constitute a set of measures source-related values. All source-related values are routed to the device via input circuits, whose essential elements include current and voltage instrument transformers, which provide necessary galvanic separation between input terminals and internal circuits. Also, they perform preliminary adaptation of the signal to features and ranges of measuring circuits inside the bay controller. Measurements of source-related values are given as digital samples. In the computer of the mainboard (**MB**), which is directly interfaced with the measurement path, samples of currents and voltages undergo initial scaling and digital processing.

The *u*REG device uses **true RMS** of currents and voltages as the information about the source value. To the highest extent possible, the RMS value represent power and energy features of the function under co-presence of fundamental frequency harmonics. The synthesis of the RMS value in *u*REG involves 50 Hz frequency harmonics, up to 13th harmonic (inclusive).

Based on the source values, derivative values are computed. These derivative values entirely correspond to **operational measurements** in the bay. They include estimated instantaneous three-phase active and reactive power values, moving average power values at 15-minute time slots and instantaneous tangent of the phase angle. Additionally, computation procedures include cumulated bidirectional active and reactive energy values in time zones, estimated loss energy in the line in time zones, peak power values in moving 15-minute time slots in time zones, cumulated bidirectional total active and reactive energy values, and average tangents of phase angles for the direction of energy outflow.

All measured source values and computed derivative values are converted to the SI units. If requested by the operator, the values can be shown on the LCD screen of the unit, and if requested by the supervisory computer, transmitted via communication interfaces as messages of computer protocols. Both direction of result presentation are independent of each other.

In order to facilitate operational duties at the protective device, and for easier testing and metrological evaluation of the device, source values and computation sections relating derivative values, are presented externally on two different scales:

- as **secondary values** expressed in units of monitored signals across device terminals (identified in the menu by the digit **3**),
- as **primary values** converted by the transformation ration on the MV or HV side (identified in the menu by the digit **4**).

While previewing measurement values in the *uREG* panel menu [section 3 and 4], measurement not available for the existing **hardware configuration** presented in grey font (this applies to **GH** and **GV** graphic panels).

In *u*REG units equipped with **GH** and **GV** graphic panels, an overall view of primary measurements values (for a definable sub-group) is made available by the basic screen → See Fig. 8.4. and screens shown in the **Mini-Monitor** mode.

In the group of settings which are directly associated with derivative computation procedures and the mode of scaling, particular attention goes to:

- setting of rated primary voltage *Un*;
- setting of rated primary voltage of zero sequence *U0n*;
- setting of primary transmission rations of phase current transformers *theta If*;
- setting of the transmission ration of the current zero sequence transformer *theta I0*, *theta Ig*;
- setting to define configuration: *star-delta*;
- setting of the active and reactive power marking change;

and

- setting of selection of time zone variant.

These settings are components of “External parameters” and “Time zones” functors.

13.1. SECONDARY MEASUREMENTS

Table 13.1. Secondary measurements

Description	Explanation and range	Notes
30 Current IL1 **31 Current IL2** **32 Current IL3**	Phase current RMS value, range: **0 – 192 [A]**	
33 Ifmax	The maximum value out of RMS phase current in IL1, IL2, IL3 – recorded to the instance of circuit-breaker activation	Signals TZ, ZW or KZ just before circuit-breaker activation reset the Ifmax state saved to that moment
34 Current I0	I0 zero current RMS value, range: **0 – 10 [A]**	
35 Current Ig	RMS zero current in the lateral branch (Ig), range: **0 – 10 [A]**	
36 Voltage U0	U0 zero voltage RMS value, range: **0 – 130 [V]**	
37 Voltage UL1 **38 Voltage UL2** **39 Voltage UL3**	Phase voltage RMS value, range: **0 – 130 [V]**	
3A Admittance Y0	Admittance of the zero sequence circuit, range: **0 – 100 [mS]**	
3B Conductance G0	Conductance of the zero sequence circuit, range: **0 – 10 [mS]**	
3C Susceptance B0	Susceptance of the zero sequence circuit range: **0 – 10 [mS]**	
3D Active power P3	Three-phase active power RMS value (1-sec.) range: **0 – 10 000 [W]**	Power value as before the sign indicating the direction of energy flow fed to busbars (+), sourced from busbars (–). Power indication is an average over 1-second period
3E Reactive power Q3	Three-phase reactive power RMS value (1-sec.) range: **0 – 10 000 [Var]**	
3F P3 15 min cz	Three-phase active power RMS (average over 15 minutes) range: **0 – 10 000 [W]**	Power calculates as a sum of marked active and reactive powers of L1, L2 and L3 busbars, multiplied by 1.5, and converted into a moving average over 15 minutes. Power indication is a negative sign in 2nd and 4th quadrant of the coordinate system.
3G Q3 15 min br	Three-phase reactive power RMS (average over 15 minutes) range: **0 – 10 000 [Var]**	
3H Frequency	Frequency **45 - 55 [Hz]**	
3I Derivative df/dt	Derivative df/dt **0.1 – 25 [Hz/s]**	
3J Voltage U12 **3K Voltage U23** **3L Voltage U31**	Line-to-line voltage RMS value, range: **0 – 130 [V]**	
3M Current Imax		
3N Current Imin		
3O Voltage Umax		
3P Voltage Umin		
3Q Voltage U0 2	Voltage U0 in section 2 [VT-2]	

3R Voltage U12 2	Line-to-line voltage U12 in section 2 [VT-2]	
3S Voltage U23 2	Line-to-line voltage U23 in section 2 [VT-2]	
3T Voltage U31 2	Line-to-line voltage U31 in section 2 [VT-2]	
3U Voltage U110 2	Voltage U110 in section 2 [VT-2]	
3V Voltage U110 1	Voltage U110 in section 2 [VT-1]	
3W Voltage U0 1	Voltage U0 in section 1 [VT-2]	
3X Voltage UL1 1	Phase voltage UL1 in section 1 [VT-2]	Repeated **37**
3Y Voltage UL2 1	Phase voltage UL2 in section 1 [VT-2]	Repeated **38**
3Z Voltage UL3 1	Phase voltage UL3 in section 1 [VT-2]	Repeated **39**
3a Voltage U12 1	Line-to-line voltage U12 in section 1 [VT-2]	Repeated **3J**
3b Voltage U23 1	Line-to-line voltage U23 in section 1 [VT-2]	Repeated **3K**
3c Voltage U31 1	Line-to-line voltage U31 in section 1 [VT-2]	Repeated **3L**
3d S1 A Voltage Uw		for MSK
3e S1 A Current Iw		
3f S1 A Angle UwIw		
3g S1 A Voltage Ud		
3h S1 A Voltage Uds		
3i S1 A Current Id		
3j S1 A Current Ids		
3k S1 B Voltage Uw		
3l S1 B Current Iw		
3m S1 B Angle UwIw		
3n S1 B Voltage Ud		
3o S1 B Voltage Uds		
3p S1 B Current Id		
3q S1 B Current Ids		
3r S2 A Voltage Uw		
3s S2 A Current Iw		
3t S2 A Angle UwIw		
3u S2 A Voltage Ud		
3v S2 A Voltage Uds		
3w S2 A Current Id		
3x S2 A Current Ids		
3y S2 B Voltage Uw		
3z S2 B Current Iw		
3- S2 B Angle UwIw		
3- S2 B Voltage Ud		
3- S2 B Voltage Uds		
3- S2 B Current Id		
3- S2 B Current Ids		
3- dU/dt		
3-Angle U0I0		

and other measurements...

13.2. PRIMARY MEASUREMENTS

Table 13.2. Primary measurements

Description	Explanation and range	Notes
40 Current IL1 **41 Current IL2** **42 Current IL3**	Phase current RMS value. Range: **0 – (lower value out of: 192*thetaIf, 10000) [A]**	
43 Current Ifmax	The maximum value of phase current RMS values in L1, L2, L3 – recorded after the last circuit-breaker activation by TZ, ZW or KZ pulse. Range: **see primary currents. IL1-IL3**	
44 Current I0	I0 zero current RMS value, Range: **0-(lower value out of: 10*theta I0, 1000)[A]**	
45 Current Ig	Current (Ig) RMS (e.g. in BKR lateral branch) Range: **0-(lower value out of: 10*theta I0, 1000)[A]**	
46 Voltage U0	Voltage RMS of zero sequence U0. Range: **0 – 130* Un/(√3*100) [kV]**	
47 Voltage UL1 **48 Voltage UL2** **49 Voltage UL3**	Phase voltage RMS value. Range: **0 – 130*Un/100 [kV]**	
4A Voltage U12 **4B Voltage U23** **4C Voltage U31**	Line-to-line voltage RMS value, Range: **0 – 130*Un/100 [kV]**	
4D Active power P3	Three-phase active power RMS (average over 1 second) – positive value with energy to the line, negative for the opposite direction. Range: **0 – 100 [MW]**	Power computed as a sum of marked busbar active power values. L1, L2 and L3
4E Reactive power Q3	Three-phase reactive power RMS value (average over 15 second) – positive value for inductive load, negative value for capacitive load. Range: **0 – 100 [Mvar]**	Power computed as a sum of marked busbar reactive power values. L1, L2 and L3
4F Frequency	Frequency **45 – 55 [Hz]**	
4G Derivative df/dt	Derivative df/dt **0.1 – 25 [Hz/s]**	
4H P3max0 15min **4J P3max1 15min** **4L P3max2 15min** **4N P3max3 15min**	Three-phase active peak-RMS power (moving average over 15 minutes), in 0th, 1st, 2nd and 3rd time zone, respectively. Range: **0 – 100 [MW]**	The determined power is an average (over 15-minute intervals – resolution --min.) peak active or reactive power value in the time zone after auxiliary power-on to the unit, or after remote register reset. **Power indication is coupled with a time marker of the maximum record.**
4I Q3max0 15min **4K Q3max1 15min** **4M Q3max2 15min** **4O Q3max3 15min**	Three-phase reactive peak-RMS power (moving average over 15 minutes), in 0th, 1st, 2nd and 3rd time zone, respectively. Range: **0 – 100 [Mvar]**	
4P Ecz+ Zone 0 **4Q Ecz+ Zone 1** **4R Ecz+ Zone 2**	Stored active energy fed to busbars in time zones. Range: **0 – 10 000 [MWh]**	Energy metered for a period of the time zone (successive days) for energy fed to busbars (Ecz+)

4S Ecz+ Zone 3		or for the direction of energy sourced from busbars (Ecz–), no backward state.
4T Ecz– Zone 0 **4U Ecz– Zone 1** **4W Ecz– Zone 2** **4X Ecz– Zone 3**	Stored active energy sourced from busbars in time zones. Range: **0 – 10 000 [MWh]**	
4Y Ebr+ Zone 0 **4Z Ebr+ Zone 1** **4a Ebr+ Zone 2** **4b Ebr+ Zone 3**	Stored reactive energy fed to busbars in time zones. Range: **0 – 10 000 [Mvarh]**	Energy metered for a period of the time zone (successive days) for energy fed to busbars (Ebr+) or for the direction of energy sourced from busbars (Ebr–), no backward state.
4c Ebr– Zone 0 **4d Ebr– Zone 1** **4e Ebr– Zone 2** **4f Ebr– Zone 3**	Stored reactive energy from busbars in time zones. Range: **0 – 10 000 [Mvarh]**	
4g Ecz+ total	Total active energy fed to busbars Range: **0 – 100 000 [MWh]**	Energy stored for the entire measurement period for the energy rate fed to busbars (Ecz+) or for energy sourced from busbars (Ecz–), no return cycles.
4h Ecz– total	Total active energy from busbars. Range: **0 – 100 000 [MWh]**	
4i Ebr+ total	Total reactive energy fed to busbars. Range: **0 – 100 000 [Mvarh]**	Energy stored for the entire measurement period for the energy rate fed to busbars (Ebz+) or for energy sourced from busbars (EBr–), no return cycles.
4j Ebr– total	Total active energy from busbars. Range: **0 – 100 000 [Mvarh]**	
4k tg(Fi) Q3/P3	Tangent of instantaneous phase angle for transformer load (with sign), calculated as the ratio of 1-second average 3-phase active and reactive power values. Range: **0 – 1000**	The maximum tangent modulus is limited to 999.99.
4l tg (Fi) Q3m/P3m	Tangent of the phase angle for transformer load (with sign), calculated as the ratio of 15-minute peak power values in the current time zone. Range: **0 – 1000**	
4m tg (Fi) zones	Average tangent of phase angle for transformer load (signed), calculated as the ratio of values of energy stored in the current time zone: reactive (Ebr+ in zone n) and active (Ecz+ in zone n) fed to busbars. Range: **0 – 1000**	
4n tg (Fi) total average	Average tangent of phase angle for transformer load (signed), calculated as the ratio of total energy values: reactive (Ebr+) and active (Ecz+) fed to busbars. Range: **0 – 1000**	
4o Σ I1 shutdowns **4p Σ I2 shutdowns** **4q Σ I3 shutdowns** **4r Σ I4 shutdowns**	Cumulated sum of RMS currents shut down by the master switch. Range: **Σ I1: 0 – Igr1*thetaIf [kA]** **Σ I2: Igr1*thetaIf – Igr2*thetaIf [kA]** **Σ I3: Igr2*thetaIf – Igr3*thetaIf [kA]** **Σ I4: Igr3*thetaIf – 192*thetaIf [kA]**, where: **Igr1 – Igr3:** circuit-breaker limit currents; **thetaIf:** transmission ratio of phase current transformers;	For the purpose of turn-off currents, the maximum value of current RMS values in L1, L2 and L3 (after a turn-off impulse is sent to the circuit-breaker coil to the moment of power cut) is used. The cumulated sum means current values converted by means of the transmission ratio into the grid primary side. The value will be stored regardless of duration of auxiliary supply interruption.
4s Resistor current	Resistor current **[kA]**	
4t Voltage U0 2	Voltage U0 in section 2 [VT-2]	
4u Voltage U12 2	Line-to-line voltage U12 in section 2 [VT-2]	
4v Voltage U23 2	Line-to-line voltage U23 in section 2 [VT-2]	
4w Voltage U31 2	Line-to-line voltage U31 in section 2 [VT-2]	

4x Voltage U110 2	Voltage U110 in section 2 [VT-2]	
4y Voltage U110 1	Voltage U110 in section 2 [VT-1]	
4z Voltage U0 1	Voltage U0 in section 1 [VT-2]	
4* Voltage UL1 1	Phase voltage UL1 in section 1 [VT-2]	Repeated **47**
4* Voltage UL2 1	Phase voltage UL2 in section 1 [VT-2]	Repeated **48**
4* Voltage UL3 1	Phase voltage UL3 in section 1 [VT-2]	Repeated **49**
4* Voltage U12 1	Line-to-line voltage U12 in section 1 [VT-2]	Repeated **4A**
4* Voltage U23 1	Line-to-line voltage U23 in section 1 [VT-2]	Repeated **4B**
4* Voltage U31 1	Line-to-line voltage U31 in section 1 [VT-2]	Repeated **4C**
4* S1 Voltage Ud		for MSK
4* S1 s		
4* S1 Ipoj		
4* S1 d0		
4* S1 Iind		
4* S1 Ireszt		
4* S2 Voltage Ud		
4* S2 s		
4* S2 Ipoj		
4* S2 d0		
4* S2 Iind		
4* S2 Ireszt		
4* Angle U0I0		
4* Current IL1 S2 [VT-3]		
4* Current IL2 S2 [VT-3]		
4* Current IL3 S2 [VT-3]		
4* cos(FI) temporary Q3|P3		

and other measurements...

14. EVENT RECORDER – REPORTS

Operation of the *u*REG protective device is associated with certain events which must be considered by operating staff. Attributes, conditions and circumstance of such events result from **the definition of the application software and the assigned indices**. The four tabs are:

- situations resulting from device operating as a protective solution (associated directly with behavior of the transformer, busbars, circuits, etc., and execution of protective criteria);
- situations affecting recognition of criterial situations (e.g. changing settings and fixing settings);
- various circumstances inside the protection, determining its instantaneous efficiency (inefficiency) as well as those which are alarming as regards continued efficiency in the immediate future.

All extraordinary situations observed during operation are saved by *u*REG in the event recorder as the so-called **reports**. Reports are collected in the caching repository in the order of creation.

The report repository of *u*REG can collect up to 1024 reports.
All reports are saved in **a non-volatile repository** – their content is stored by the period of auxiliary voltage dip.

Ongoing readout of event reports from the device should be performed by the supervisory system, e.g. a substation hub.

Previewing recorded reports is possible by means of keyboard operations using the local LCD screen or remotely via readout commands sent from the computer.

14.1. REPORTS – PREVIEW THOUGH *u*REG MENU

The reports are accessible on the main level [ident 6 '**Reports**'] in the menu structure of the LCD screen. Report presentation is subject to a rule stating that each step into the report structure results in automatic report renumbering. With this solution, **reports are always presented from the earliest report**, which is assigned with the number 00.

- The reports shown on the alphanumeric display of the unit equipped with an **NV** panel present:
  - report no.;
  - event code (as a hexadecimal protocol index, e.g. DNP-3);
  - time marker given as date and time when recorded (for milliseconds);
  - microsecond extension of the time marker (accuracy up to 100 us).

  Example:

```
02 000E 11.06.01
 11:47:30.888 1
```

→ report no. 2, code 000Eh = 14, date 2011.06.01, hour 11:47:30.888 + 100us.

- For units equipped with a color **GH/GV** graphic display, viewing event reports has three options:

1. **Three last** (earliest) reports are <u>always</u> presented on the main screen, whereas the last report is always highlighted, e.g.:

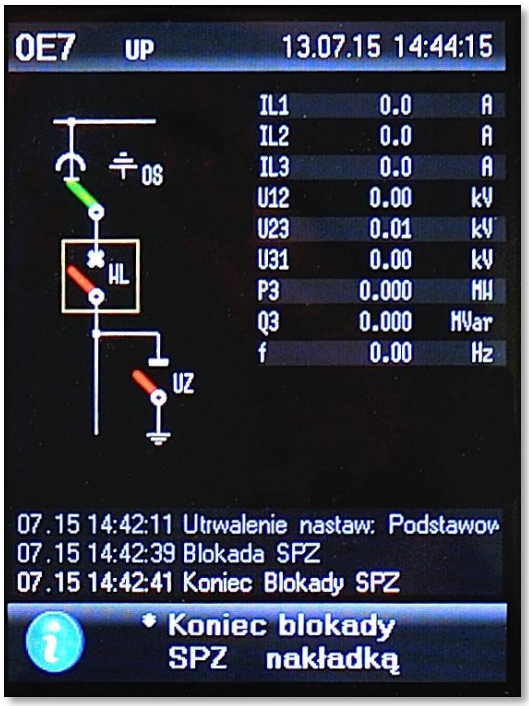


Fig. 14.1. Reports on the main screen of graphic panels.

This mode of report presentation has the following format:

mm.dd gg:mm:ss report extended description

where mm.dd – month.day, gg:mm:ss – hours.minutes.seconds.

2. Report viewing through the menu structure [ident 6 '**Reports**']. Report presentation is similar to the mode of NV panels, i.e.:

- report no.;
- event code (as a hexadecimal index, e.g. DNP-3);
- time marker given as date and time when recorded (for milliseconds);
- microsecond extension of the time marker (accuracy up to 100 us), and additionally:
- extended report description (the so-called extended report).

Example:

09.0112:11.06.01 12:32:24.331 4
W2 low state

→ report no. 9, code 0112h = 274, date 2011.06.01, hour 12:32:24.331 + 400us.

Viewed reports are displayed in yellow.

3. Report viewing through **Event reports** in **Mini-Monitor** mode.

Max. 63 reports can be displayed (from the last auxiliary power-up). Reports can be scrolled by pressing ▼ ▲. Report presentation is given in the table form (8 pcs) with the format discussed in → 2.

14.2. REPORTS – PREVIEW THOUGH THE APPLICATION SOFTWARE

*u*REG is supplied with *Monitor3* – a PC program – to provide a quick and convenient access to reports, together with their full interpretation (resulting from the defined device **APPLICATION**).

Report presentation in the program follows the following scheme:

- time marker given as date and time when recorded (for milliseconds);
- microsecond extension of the time marker (accuracy up to 100 us for uCZIPstd protocol, and up to 1 ms for DNP-3 and IEC-60870-5-10X protocols);
- event code (as a hexadecimal protocol index, e.g. DNP-3);
- report brief description (the so-called brief report);
- no. of the functor generating the report;
- extended report description (the so-called extended report).
- optional measured value associated with the report

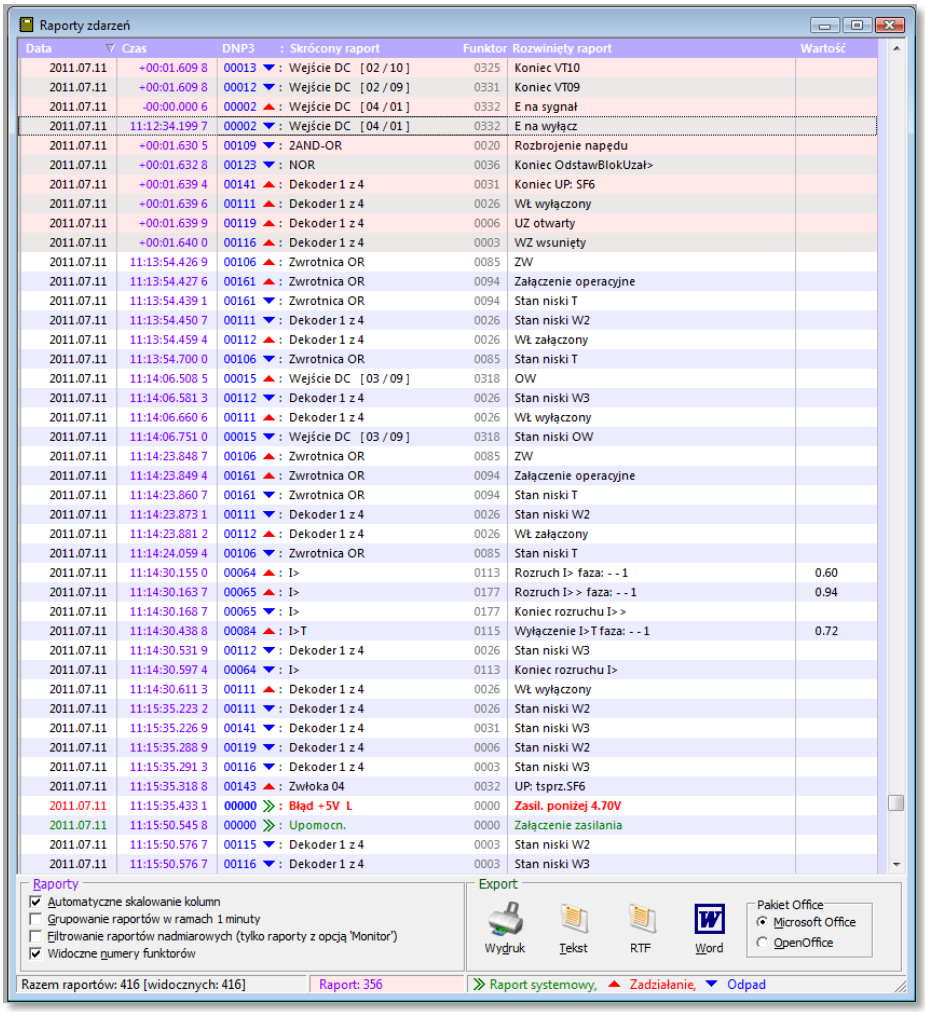


Fig. 14.2. Event Reports windows in *Monitor3*.

Reports can be grouped, filtered and exported to external files.

CAUTION:

*The range (number) of reports, event code assignment (DNP-3 indices) in the reports, report texts and their color scheme presented in Monitor3 are strictly defined in the **APPLICATION** in the LogCZIP system.*

14.3. SYSTEM REPORTS

The *u*REG system has a special group of reports – **System reports** – whose code (index) is = 0, identified by a DEC or HEX marker. These reports cannot be redefined by the user (at the stage of *Log*CZIP application development) and are used to indicate malfunctions of the units and its improper settings.
The key to event codes in system reports is presented in Table 14.3.

Table 14.3.

Attribute DEC	Attribute HEX	Meaning
0	0	Undefined system report
1	1	Uaux → Auxiliary power-up and start of initial calibration procedure
2	2	Uaux → Power off
…	…	Reserved
24	18	Failed settings → Error in main settings
25	19	Failed settings → Error in standby settings
26	1 A	Failed settings → Error in auxiliary settings (Transmission + LCD)
…	…	Reserved
32	20	Implementation of I2C bus (indication of I2C bus on LCD screen, slot in Reports)
33	21	Fixing settings: Main
34	22	Fixing settings: Backup
35	23	Change bank of settings: Main → Standby
36	24	Change bank of settings: Standby → Main
37	25	Fixing settings: Auxiliary (Transmission + LCD)
38	26	Fix corrections
…	…	Reserved
48	30	Error of relays
…	…	Reserved
56	38	Exceeded 1st threshold for maximum temperature inside the enclosure
…	…	Reserved
64	40	Fault of LEDs
…	…	Reserved
72	48	Fault of LCD screen
…	…	Reserved
80	50	Fault of relays → Improper current of relays
…	…	Reserved
88	58	Failed reports → Faulty readout of reports
…	…	Reserved
96	60	Supply +5V back to normal
97	61	Failed +5V → Supply below 4.70 V
98	62	Failed +5V → First instance of exceeded supply voltage +5 V beyond allowable range 4.75 – 5.25 V
99	63	Failed +5V → Supply below 4.55 V
100	64	Failed +1.8V → Supply of IF module below +1.75 V
101	65	Failed +1.8V → Supply of IF module below +1.85 V
102	66	Failed +5 V → Panel supply below +4.75 V
103	67	Failed +5V → Panel supply exceeds +5.25 V
104	68	Failed +12V → Panel supply below +10 V
105	69	Failed +12V → Panel supply exceeds +14 V
106	6 A	Panel temperature below normal
107	6B	Panel temperature exceeded Display backlight will be turned off.

		Backlight will be resumed automatically when the display is cooled down.
…	…	Reserved
112	70	Failed +5V → Motherboard (MB) supply below +4.75 V
113	71	Failed +5V → Motherboard (MB) supply exceeds +5.25 V
114	72	Failed +3.3V → Motherboard (MB) supply below +3.20 V
115	73	Failed +3.3V → Motherboard (MB) supply exceeds +3.40 V
116	74	Failed -12V → Motherboard (MB) supply below -14 V
117	75	Failed -12V → Motherboard (MB) supply exceeds -10 V
118	76	Failed +12V → Motherboard (MB) supply below +10 V
119	77	Failed +12V → Motherboard (MB) supply exceeds +14 V
120	78	Motherboard (MB) temperature below normal
121	79	Motherboard (MB) temperature exceeded Display backlight will be turned off. Backlight will be resumed automatically when the display is cooled down.
…	…	Reserved
128	80	Failed counters → Faulty readout of counters
129	81	Missing SLOTOCCUP → Failed collection of module configuration
130	82	Netlist error → Failed Netlist initialization
131	83	Failed SLOTOCCUP → Incompatibility between module configuration and application
132	84	Failed SPI → Failed SPI bus – No communication with MB
133	85	MB fault → MB Hard fault exception
…	…	Reserved

15. DATA RECORDERS

15.1. DAR - Digital and Analog Recorder

All *u*REG units are equipped with an additional current / voltage / digital data recorder located in the IF-x module (also referred to as the **disturbance recorder**), which is associated with selected events affecting protective decisions.

The recorder memory is divided into buffers.

Each buffer always records 10 electrical values:

→ Configuration with VT-0
1 set of voltages and currents
- Voltage U1;
- Current I1;
- Voltage U2;
- Current I2;
- Voltage U3;
- Current I3;
- Voltage U0;
- Current I0;
- AUXI0 input (VT);
- Current Ig;

→ Configuration with VT-2/VT-1
2 sets of voltages, 1 set of currents+I0
- Voltage U1_1;
- Current I1;
- Voltage U2_1;
- Current I2;
- Voltage U3_1;
- Current I3;
- Voltage U0_1;
- Current I0;
- Voltage U1_2;
- Voltage U0_2;

→ Configuration with VT-3/VT-4
2 sets of voltages, 2 sets of currents
- Voltage U1_1;
- Current I1_1;
- Voltage U2_1;
- Current I2_1;
- Voltage U3_1;
- Current I3_1;
- Current I3_2;
- Current I1_2;
- Voltage U1_2;
- Current I2_2;

and **96 digital states** (outputs of functors → see ***Log*CZIP APPLICATION**).

Data are recorded in buffers in numerals (the so-called samples) with at a **standard frequency of 1600 Hz – 32 samples per period** for each data set, according to the monitored values directly at device terminals.

Available for each version of the **IF-x** module, the recorder memory can be configured to support up to 10, 11 to 19 or even several tens buffers of different capacity.

In a standard solution, the following **configurations** of recorder buffers are available at 1600 Hz – **[IF-0 4MB] / [IF-4 8/16MB]**:

- 2*20.48 s (2 buffers, 20.48 s each),
- 4*10.24 s,
- 8*5.12 s,
- 16*2.56 s,
- 32*1.28 s,
- 2*40.96 s,
- 4*20.48 s,
- 8*10.24 s,
- 16*5.12 s,
- 32*2.56 s.

Additionally, the range of buffer configuration in the **IF-4 [8/16 MB]** module is **extended over the following settings**:

- 2*81.92 s,
- 4*40.96 s,
- 8*20.48 s,

- 16*10.24 s,
- 32*5.12 s.

In addition, the **IF-4** module combined with the **MB-2 or MB-3** motherboard provides a data recorder operated at **3200 Hz (64 samples per period)** and recording of up to **192 digital states**.

Optionally, the following additional settings can be declared in the **IF-4 [32 MB] module (mode 3200 Hz)**:

- 2*163.84 s,
- 4*81.92 s,
- 8*40.96 s,
- 16*20.48 s,
- 32*10.24 s.

Each buffer is a cyclic register and can assume one of two states: empty buffer or full buffer. Once the empty buffer is selected, recording is taking place continuously from initiation (for any period of time) to latch activation. The latch stops recording in the buffer, which has been active so far, and changes its state to 'full'. Then the local computer selects another empty buffer and initiates recording.

The procedure for selecting the recording buffer becomes complicated when all buffers are full, but another buffer must be selected for data logging. The solution in this situation depends on the user's preferences as defined in '**Overwriting mode**'.

The following options are available:

- unconditional permission to overwrite (always **overwrite**), which means a permission to change the state of the buffer with the oldest records (and irreversible deletion) into an empty buffer. If this is the case, **one buffer is always empty** and recording is continuous. This method is recommended for a high number of buffers.
- complete prohibition to overwrite (never **overwrite**) – once all buffer are filled, the recorder is turned off. Recording can be resumed only after buffers are reset (remote operation). In *uREG* units equipped with **GH**/**GV** graphic display panels, the full state of all buffers is additionally signaled by the icon  .

Functionality of the data recorder, rules of division into buffers and their handling are fully defined in the system functor – REJESTRATOR. The REJESTRATOR function has to settings ('**configuration of buffers**' and '**overwriting mode**') determines how to handle buffers.

The functor has two groups of latch activating inputs: inputs executing the latch function by a rising edge (0 – 3) and inputs executing the latch function by a falling edge (4 – 7). As for the source of latch signals, there are outputs to other functors (generating latch events) tied to selected recorder inputs.

Latching events usually include shutdown decision and some excitations without direct shutdown.

For shutting-down events, it is recommended to activate the latch using a falling edge of OFF signal; then, recording includes the shutdown process and current decay.

For non-OFF events, the latch may follow a delay (if defined in **APPLICATION**) and can be lagged against the event by any definable time slice (depending on the delay value). It is more reasonable to latch such events using a rising edge of signal.

The nature of OFF and non-OFF events results from the description developed in the **APPLICATION**. Thus, these may include:

- trip-out by protection (also by operational protection),
- trip-out by LRW,
- functional switching (ZW, KZ, TZ),
- activation by ATS,
- voltage protection,
- frequency protection,
- earth fault (EI, EU).
- overloading,
- and any other.

Logged data are analyzed using *Monitor3* with integrated support of *Data Recorder*. The program can be used to read out, view and analyze data collected in buffers, permanent storage of such data (archiving), export/import (COMTRADE) and buffer management reconfiguration, resetting, latch operations, etc.). Read buffers can be secondarily visualized in the *LogCZIP* editor (function: digital data recording analysis).

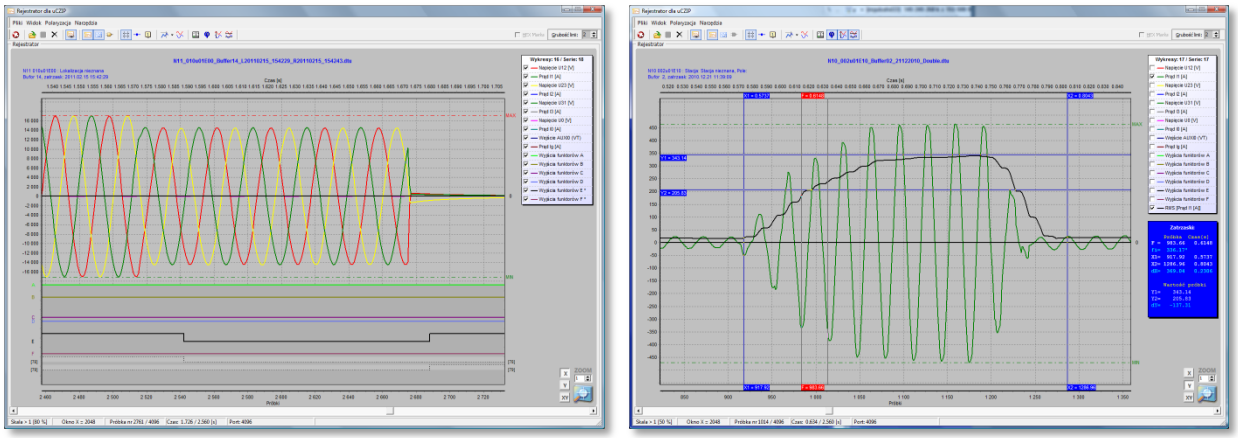


Fig. 15.1. Example screen of Data Recorder in *Monitor3*.

15.2. CDAR - Criterial RMS Recorder

All *u*REG applications can be equipped with an additional RMS criterial recorder, defined in the system functor – REJESTRATOR KRYTERIALNY. The functor supports non-volatile flash based recording up to 32 configurable buffers of data. For each of the buffers the user can choose max. 16 RMS values to be recorded (from the secondary measurements list). The RMS values will be recorded according to '**Storage frequency**' setting. Logged data are analyzed using *Monitor3* with integrated support of *Criterial Data Recorder*. The program can be used to read out, view and analyze data collected in buffers, permanent storage of such data (archiving), export/import (COMTRADE) and buffer management – similar as above.

16. COMMUNICATION

*u*REG units are equipped with a full set of the most common communication interfaces, i.e.:

- accessible in the link panel: (see → 8. Operator panel)
  - **RS 232** serial (acc. to definitions of EIA RS-232C),
  - **USB 2.0** (Universal Serial Bus);

- accessible in the IF-x module of the link: (see → 7.1. IF-x module)
  - Ethernet (network link) 10/100BASE-T **ETH**,
  - basic serial **RS-485 in** standard **RS-485** (RS-422),
  - auxiliary serial **AUX-485 in** standard **RS-485** (RS-422),
  - serial (panel) **PANEL** in standard **RS-485**.

CAUTION:
All communication interfaces are provided with full galvanic insulation (except USB).

16.1. GENERAL COMMUNICATION RULES

Information interchange via communication links takes place during normal operation of the device and does not limit any functions.

uREG communication features depend on the interface type and the corresponding protocol selected. In each single case, *uREG* communicates with a supervisory computer system via serial data transmission, simultaneously in both directions (full-duplex) or in one direction at a time (half-duplex).

For transmission protocols via Ethernet, the connection is established according to general rules conforming to relevant standards. With the intended use of the device, it is recommended to use the device within private local networks.

For protocols using RS485 interface, *uREG* does not initiate transmission (except special cases). The task to establish and maintain communication is delegated to the supervisory system, whereas *uREG* waits for an incoming message with instructions. Therefore, the device monitors the receiving line in each active interface to accept the message and immediately sends a response (once ready) to the transmission line of the same interface.

16.1.1. RS-232 INTERFACE

Information interchange via **RS 232** (EIA RS-232C) uses a **5-line** link with a subset of signal for direct operation together with a PC, modem, or alternatively, another supervisory system.
RS 232 interface lines are arranged in a **DB9M** connector (male):

- **RxD** **pin 2** - Received data
- **TxD** **pin 3** - Transmitted data,
- **RTS** **pin 7** - Request to Send,
- **CTS** **pin 8** - Clear to Send,
- **SG** **pin 5** - Ground,
- **PI** **pin 6** - Pin-in,
- **PO** **pin 1** - Pin-out.

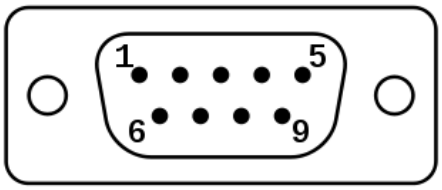


Fig. 16.1.1. DB9M connector for RS 232 interface.

The RS 232 connector has galvanic separation.

CAUTION:

Pin 1 (PO) and pin 6 (PI) must be shorted in an external plug of the connecting cable. (These pins are used to close the local interface power circuit when being connected to the computer). It is not allowed to connect up pins 1 and 6 to other circuits.

RS 232 interface is designed by data interchange in full-duplex or half-duplex, and principally in the end-to-end topology.
Code-oriented transmission parameters such as baud speed, parity bit selection and duplex range are to be programmed by means of settings (→ 1 **Auxiliary settings** → 11 **UART communication**).

Baud rate can be programmed within the range 300 to 115200 baud, which is common for both directions of transmission directions. Transmitted characters are entirely in the 8-bit ASCII set. If character-oriented parity check is applied, in the 9th bit position, it can be zero's complement (even parity) or one's complement (odd parity). The interface can also serve its purpose without parity check (no parity). The number of stop bits is fixed. Information interchange is performed as defined for the protocols: *uCZIPstd* or *uCZIPnet*.

Factory settings* of the RS-232 connector → 19 200 Bd, parity, full duplex, *uCZIPstd* protocol.
* – Conformity with default settings of CZIP and CZIP-1,2,3,4 units.

16.1.2. USB INTERFACE (B-type)

The Universal Serial Bus (USB) provides communication with an external PC (e.g. laptop/notebook) using a standard cable with A-type pins (from the PC side) and B-type pins (from the *u*REG side).

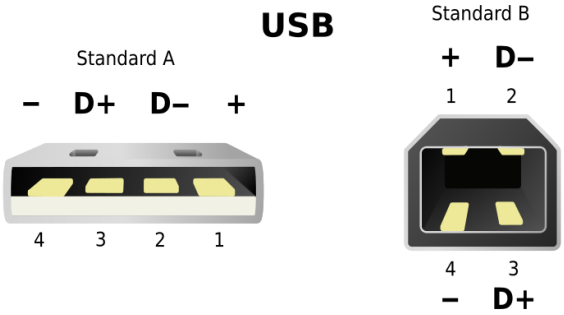


Fig. 16.1.2. Wiring diagram of USB interface.

- **V_{BUS}** **pin 1** - supply +5 V (max 0.5 A),
- **D-** **pin 2** - Data D-,
- **D+** **pin 3** - Data D+,
- **GND** **pin 4** - Ground.

Transmission can be executed during normal functioning of the unit.
*u*REG is recognized by MS Windows (compatible with NT - XP, Vista, 7, 8.1 or higher) as HID (*Human Interface Device*) and requires no installation of any additional drivers on the system! The USB connector is also not associated with any setting in the *u*REG unit.

USB communication is always performed by *uCZIP*std which, additionally, is indicated by icon on **GH**/**GV** graphic panels.

16.1.3. RS-485 /AUX-485 INTERFACES

All **RS-485** communication interfaces of the device with an IF-0 module manufactured as a **4-wire link** as standard. Thus, each interface can exchange data in full-duplex.

RS-485 interface lines are arranged in a **DB9F** connector (female) as follows:

- **A** **pin 8** - Data Input (+)
- **B** **pin 7** - Data Input (–)
- **Y** **pin 2** - Data Output (+),
- **Z** **pin 3** - Data Output (–).

The 4-wire interface can be externally reduced to a 2-wire configuration by shorting A and Y and B with Z in pairs (e.g. in the cable pin). In this case, half-duplex is the only possible exchange mode.

In both cases, the supervisory system can be linked with many *u*REG units as slave nodes; however, non-simultaneous exchange is principally less effective and loads the interface message processor to a greater extent.

The interface has no external signals controlling the direction of information flow. Bus mastering by the unit's transmitter occurs after a respond to the received message is ready. The bus is released one the last stop bit is transmitted. Efficiency of bus mastering and correct transmission is controlled by the unit's circuits.

Code-oriented transmission parameters, i.e. baud speed, parity bit selection, duplex range are to be programmed by means of settings (→ 1 **Auxiliary settings** → 11 **UART communication**); Speed range: 300 ÷ 512000 Bd.

CAUTION:

In order to switch from full-duplex to half-duplex, it is required to bridge pins 8 with 2 and 7 with 3 in DB9M complementary plug.
A reverse operation is not possible.

For the IF-1 (IF-2) module, RS-485 (and AUX-485) interface(s) are adapted to communicate via optical fiber cables (***FO*** – ***f***iber ***o***ptic) based on plastic (POF 660 nm)
or glass (G 62.5/125 880 nm) fibers.

Information interchange through RS-485 and AUX-485 interfaces can be provided by definition via **one of several transmission protocols** (selectable by **Protocol** setting) from the list:

- *uCZIPstd* (standard),
- *uCZIPnet*,
- DNP 3,
- IEC 60870-5-101,
- IEC 60870-5-103,
- CZIPstd (backward compatibility),
- CAN-PPM2 (IF-3/IF-4),
- *uCZIPstd* Master /for ATS/
- MCZIPStd (Master CZIPstd backward compatibility),
- Modbus RTU Slave,
- Modbus ASCII Slave,
- Modbus RTU Master.

CAUTION:

Each change in the setting must be applied by momentary disconnection and reconnection of auxiliary power.

Factory settings of RS-485/AUX-485 connectors are as follows:
→ 115200 Bd, no parity, 2 stop bits, full-duplex, *uCZIP*std protocol.

16.1.4. PN-485 INTERFACE (PANEL)

As already mentioned, the operator panel in *u*REG can be operated remotely → connected to the central unit by a cable with a length up to 15 m.
Communication involves a separated **RS-485** interface which is symmetrically reproduced on three side of the IF-x module (installation options → see 7 Modules and 8 Panel).

PN-485 interface lines are arranged in a **9-wireDB9F** connector (female) as follows:

- **+12V** **pin 1** - panel supply,
- **GND** **pin 5** - ground,
- **-12V** **pin 6** - panel supply,
- **Internal** **pin 4** - for internal use,,
- **+3.3 V** **pin 9** - panel supply

- **A** **pin 8** - Data Input (+),
- **B** **pin 7** - Data Input (–),
- **Y** **pin 2** - Data Output (+),
- **Z** **pin 3** - Data Output (–).

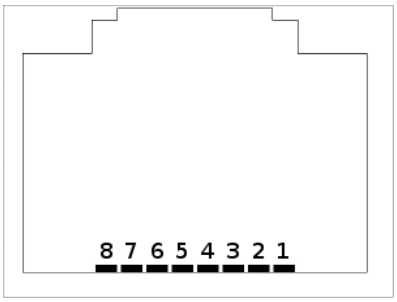
Transmission parameters and the data interchange protocol are specified by firmware and are not to be tampered with by the user.

Communication with the panel can be disabled using the administrator's setting **Disable panel** in **Auxiliary settings** (via *Monitor3*). Then, the device able to work without the panel (panel presence in the system will not be checked or reported).

CAUTION:
Each change in the setting must be applied by momentary disconnection and reconnection of auxiliary power.

16.1.5. ETHERNET (ETH) INTERFACE

*u*REG is equipped with an insulated Ethernet 10/100BASE-T interface with a standard 8P8C (i.e. RJ-45) port, which has two LEDs to indicate link and activity of the interface. Additionally, port activity is signaled by icon on **GH**/**GV** graphic panels.



Pin	Name	Direction	Description
1	Rx+	IN	Received data (+)
2	Rx–	IN	Transmitted data (–)
3	Tx+	OUT	Transmitted data (+)
4	NC		
5	NC		
6	Tx–	OUT	Transmitted data (–)
7	NC		
8	NC		

Fig. 16.1.5.1. Wiring diagram of Ethernet port.

TCP/IP model divides network communication into some layers operating with one another (i.e. ISO OSI model). Each layer requires a specific protocol.

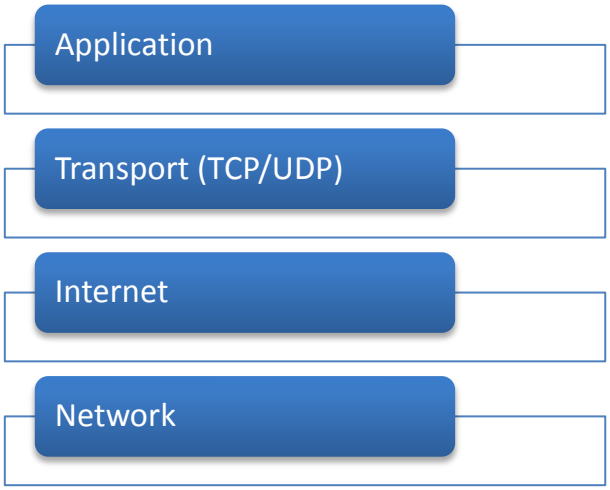


Fig. 16.1.5.2. TCP/IP layers

IP stack application layer is the highest level for services such as WWW server, FTP, SMTP. Also, it includes a set of transmission protocols used by external programs to communicate with *u*REG.

The **ETH** interface in *u*REG has the following protocols implemented:

- uCZIPstd – TCP or UDP transport layer,
- DNP-3 – TCP or UDP transport layer,
- IEC-60870-5-104,
- IEEE-1588 - PTP time synchronization: precision = 1 µs,
- Modbus TCP (slave/master), other.

Also, both **ETH** and *u*REG are adapted to handle a later **IEC-61850** protocol (*real time Ethernet*).

For standard versions of the device, MAC address is fixed at factory to prepare the device for use within private local networks. If necessary to connect the device to the public network, it is recommended to contact technical staff at *REGULUS* to register a global address.

16.2. COMMUNICATION SETTINGS

Communication settings are saves in the **auxiliary settings** bank and are always accessible via *Monitor3*, even if the device has no **APPLICATION**)!

Menu in *u*REG has a group of auxiliary settings divided in two sub-groups of transmission settings: '**11 UART communication**' and '**12 Ethernet communication**'.

The setting sub-group **UART communication** contains 24 settings to program transmission parameters of serial interfaces, i.e. RS-232, RS-485 and AUX-485. All settings in the sub-group (once fixed) define default values, i.e. values activated automatically and every time after starting and restarting the device and after restoring the settings.

The setting sub-group **Ethernet communication** contains 21 settings to program network transmission parameters. All settings in the sub-group (once fixed) define default values, i.e. values activated automatically and every time after starting and restarting the device and after restoring the settings.

The settings are listed in Tables 16.2.1. and 16.2.2.
Default settings are in bold; these are activated after first auxiliary power-up and until their first modification (also, if settings is corrupted).

CAUTION:

*While working with Monitor3 (in the window of Auxiliary settings), all transmission settings are all presented in one group (division into interface sub-groups **UART** and **Ethernet** have a distinct background color) and numbered 1÷53.*

Settings no. 25 to 32 refer to panel interface (PN-485) and are reserved (Administrator mode).

CAUTION:

Changing the settings of:

- *Ethernet port,*
- *protocol for 485/FO interface,*
- *BTS setting to achieve [Port DISABLED]*

requires their activation, and uREG must be restarted!

Table 16.2.1. Communication settings (UART communication)

Setting designation and description	Denomination IDENT in menu	Setting value
RS232 activity signal used to signal interface activity by the LED (on the panel)	110 Active signal RS232	**active**, inactive
RS-232 baud speed: transmission speed via RS232 links	111 Baud speed for RS-232	300, 600, 1200, 2400, 4800, 9600, **19200**, 23300, 28800, 38400, 57600, 115200
Parity bit RS-232: used to set the mode of code-oriented transmission control	112 Parity bit RS232	none, **even parity,** odd parity
Duplex RS-232: used to set bidirectional simultaneity of transmission	113 Duplex RS232	half, **full**
Logic number RS-232: two-digit individual address of the device to make it explicitly distinguishable among devices connected to the common computer bus. The number is attached to messages sent to/from the master computer to specify the message recipient.	114 Logic number RS-232:	0 – 99 default **1**
RS-232 protocol: type of interface transmission protocol	115 Protocol RS232	**uCZIPstd** uCZIPnet
RS485 activity signal used to signal interface activity by the LED (when ON and on the panel)	116 Active signal RS485	**active**, inactive
Baud speed RS485/FO1: transmission speed via interface links	117 Baud speed for RS-485	300, 600, 1200, 2400, 4800, 9600, 19200, 28800, 38400, 57600, 76800, **115200**, 138240.1728, 230400, 256000.460800, 512000, CAN 25 kbs, CAN 125 kbps
Parity bit RS485/FO1: used to set the mode of code-oriented transmission control	118 Parity bit RS485	even parity, odd parity, **none**
Stop bits RS485/FO1:	119 Stop bits RS485	1 bit, **2 bits**
Duplex RS485/FO1: used to set bidirectional simultaneity of transmission	11A Duplex RS485	half, **full,** FOring.non-light, FOring.light, FO.radius.non-light, FOradius.light
Logic number RS485/FO1 (younger): individual (16-bit MSB|LSB) address of the device to make it distinguishable among devices connected to the common computer bus. The number is attached to messages sent to/from the master computer to specify the message recipient.	11B Logic number (LSB) RS-485	0 – 255 default **1**
Logic number RS485/FO1 (older):	11C Logic number (MSB) RS-485	0 – 255 default **0**
Protocol RS485/FO1: type of interface transmission protocol	11D Protocol RS485	**uCZIPstd**, uCZIPnet,DNP3, IEC 60870-5-101, IEC 60870-5-103, CZIPstd, CAN-PPM2, uCZIPstd MASTER, MCZIPStd, Modbus RTU Slave, Modbus ASCII Slave, Master Modbus RTU
BTS interlock for RS485/FO1: used to activate interlock of telecontrol via RS485/FO1	11E BTS interlock for RS485	**inactive BTS,** active BTS, Port DISABLED

AUX485 activity signal: used to signal interface activity by the LED (when ON and on the panel)	11F Activity signal AX485	**active**, inactive
Baud speed for AUX485/FO2: transmission speed via interface links	11G Baud speed for AX485	300, 600, 1200, 2400, 4800, 9600, 19200, 28800, 38400, 57600, 76800, **115200**, 138240.1728, 230400, 256000.460800, 512000, CAN 25 kbs, CAN 125 kbps
Parity bit AUX485/FO2: used to set the mode of code-oriented transmission control	11H Parity bit AX485	even parity, odd parity, **none**
Stop bits AUX485/FO2:	11I Stop bits AX485	1 bit, **2 bits**
Duplex AUX485/FO2: used to set bidirectional simultaneity of transmission	11J Duplex AX485	half, **full,** Fook.non-light, Fook.light, Fopr.non-light, Fopr.light
Logic number AUX485/FO2 (younger): individual (16-bit MSB|LSB) address of the device to make it distinguishable among devices connected to the common computer bus. The number is attached to messages sent to/from the master computer to specify the message recipient.	11K Logic number (LSB) AX485	0 – 255 default **1**
Logic number AUX485/FO2 (older):	11L Logic number (MSB) AX485	0 – 255 default **0**
Protocol AUX485/FO2: type of interface transmission protocol	11M Protocol AX485	**uCZIPstd**, uCZIPnet,DNP3, IEC 60870-5-101, IEC 60870-5-103, CZIPstd, CAN-PPM2, uCZIPstd MASTER, MCZIPStd, Modbus RTU Slave, Modbus ASCII Slave, Master Modbus RTU
BTS interlock for RS485/FO2: used to activate interlock of telecontrol via AX485/FO2	11N BTS interlock for AX485	**inactive BTS,** active BTS, Port DISABLED

Table 16.2.2. Communication settings (Ethernet communication).

Setting designation and description	Denomination	Setting value
IP address element 1 (MSB): IP address of Ethernet interface of uREG	120 IP address element (1)	0 – 255 default **192**
IP address element 2	121 IP address element (2)	0 – 255 default **168**
IP address element 3	122 IP address element (3)	0 – 255 default **1**
IP address element 4 (LSB)	123 IP address element (4)	0 – 255 default **100**
IP mask element 1 (MSB): IP mask of Ethernet interface of uREG	124 IP mask element (1)	0 – 255 default **255**
IP mask element 2	125 IP mask element (2)	0 – 255 default **255**
IP mask element 3	126 IP mask element (3)	0 – 255 default **255**
IP mask element 4 (LSB)	127 IP mask element (4)	0 – 255 default **0**
IP gateway element 1 (MSB) Router IP address	128 IP gateway element (1)	0 – 255 default **192**
IP gateway element 2	129 IP gateway element (2)	0 – 255 default **168**
IP gateway element 3	12A IP gateway element (3)	0 – 255 default **1**
IP gateway element 4 (LSB)	12B IP gateway element (4)	0 – 255 default **1**
IP port (uCZIPStd protocol) MSB 16-bit number of IP port of 2 x bytes (MSB|LSB) for decimal definition, e.g. 15|162 = 0FA2h = 4002	12C Prot.uCZIPStd Port MSB	0 – 255 default **15 = 0Fh**
IP port (uCZIPStd protocol) LSB	12D Prot.uCZIPStd Port LSB	0 – 255 **default 162 = A2h**
IP port (DNP-3 protocol) MSB	12E Prot.DNP-3 Port MSB	0 – 255 default **15**
IP port (DNP-3 protocol) LSB	12F Prot.DNP-3 Port LSB	0 – 255 default **162**
Transport layer	12G Transport layer	**UDP- STD DNP3**, TCP- STD DNP3, UDP-STD | TCP-DNP3, TCP-STD | UDP-DNP3, UDP-STD | TCP-104, TCP-STD | TCP-104, TCP-104 | TCP-104, UDP-STD MDNP3, Modbus TCP | Modbus TCP, Modbus TCP | DNP3, UDP DNP3 | Master DNP3, UDP DNP3 | Master Modbus UDP DNP3 | TCP DNP3 SCADA, TCP DNP3 | UDP DNP3 SCADA
Activation of public MAC address Reserved setting	12H Public MAC address	**inactive,** active
IEEE 1588 PTP Mode during synchronization of clock by IEEE 1588 protocol, In **Master** option, **one** of uREG units become the synchronizer.	12I IEEE 1588 PTP	**slave**, master
BTS interlock for TCP: Used to activate interlock of telecontrol via ETH (in TCP protocol)	12J BTS interlock for TCP	**inactive BTS,** active BTS, Port DISABLED
BTS interlock for UDP: Used to activate interlock of telecontrol via ETH (in UDP protocol)	12K BTS interlock for UDP	**inactive BTS,** active BTS, Port DISABLED

MSB – most significant byte.
LSB – least significant byte.

17. TESTS AND EVALUATION OF PERFORMANCE

17.1. TEST CLASSIFICATION

uREG contains circuits and software for evaluating its performance and maintaining its readiness for operation. Test equipment and procedures are divided into five categories:

- **Initial performance test (when started):**

POST procedures (power on self test - initial performance testing) inspect local and peripheral hardware. If the test fails at this stage, the device will be immediately restarted and the test will be repeated. If the defect is permanent, these operations will be repeated infinitely. Performance confirmed during the test is required to continue the starting procedure.

- **Periodic testing and performance monitoring:**

During normal operation, hierarchic procedures for periodic testing are activated. The scope of the testing during operation is limited to actions which do not conflict with main protective functions. Regular monitoring applies to: supply source, semantic correctness and information interchange follow-up to confirm working order of computers, relay control circuits, bus components, program memory and the panel (LEDs, display). For some main protective operations, maximum times are set. If these times are exceeded, the device is recognized as faulty.

- **Routine calibration and controlled circuit adjustment:**

The measurement path is subject to regular testing during operation of the protective device. Apart from the check, continuous calibration circuits are activated as well. The calibration mechanism is based on statistical quality evaluation of the path and automatic application of a corrective value. A persistently exceeded deviation (after two attempts) beyond the adjustment range is the reason to recognize the path as faulty.

- **Failure alarms and failure recovery**

Device activity (at the highest test hierarchy level) is checked by a special hardware-based supervision system (the so-called watch-dog). The watch-dog requires that procedures of the directly lower hierarchy should systematically confirm their ‘presence’ and ‘capability’. Failed requests – caused by power failure or software self-lock – resulting in an immediate action to restore normal operation of the system. If damage to an element is recognized by systems and procedures in the mentioned categories, an error is alarmed and an attempt to resume a normal state of the device is initiated.

- **On-demand performance tests of selected resources:**

The fifth group refers to operational checks performed when requested by the operator, who is responsible for evaluating the tested circuit. For example, this kind of check may concern LEDs.

17.2. MEASURED INTERNAL PARAMETERS

Some measurements and results of ancillary test procedures can be read out by the operator. These values are accessible through the menu information structure in the group '**5 Tests**', in the sub-group '**50 Internal parameters**'.

Explanation of test measurements, the description on the display and assumed ranges are presented in the following table.

Table 17.2. Internal parameters.

Description	Meaning	Range
500 IF +5	Control voltage +5V of the IF board power unit for internal alarms of expected power failure	0 – 5.50 [V]
501 IF +1.8	Control voltage +1.80V of the IF board power unit	0 – 3.00 [V]
502 MB +5	Control voltage +5V of the MB power unit	0 – 5.50 [V]
503 MB +3.3	Control voltage +3.30V of the MB power unit	0 – 4.00 [V]
504 MB +12	Control voltage +12V of the MB power unit	0 – 15.0 [V]
505 MB -12	Control voltage -12V of the MB power unit	0 – -15.0 [V]
506 MB temp.	MB internal temperature	0 – 100 [°C]
507 Panel +5	Control voltage +5V of the panel power unit	0 – 5.50 [V]
508 Panel +12	Control voltage +12V of the panel power unit	0 – 15.0 [V]
509 Panel temp.	Panel board internal temperature	0 – 100 [°C]

17.3. ON-DEMAND TESTS

17.3.1. LED TEST

LED test (ident 51) is aimed to confirm quickly good working order of LEDs. The test is initiated by pressing ▼ on the first attempt.

The LED test has four stages as follows:

1. lighting up programmable LEDs → first 8 red LEDs and 8 green LEDs (NV),
   → first 16 red LEDs (GH, GV);
2. lighting up other programmable LEDs (as regards POWER, FAILURE, UP)
3. turning LEDs off;
4. lighting up all LEDs and lighting up LEDs as before the test.

CAUTION:
The LED test does not cover the BTS diode and the diode indicating serial interface transmission.

17.3.2. SERIAL NUMBER

Serial number (ident 52) assigned to *u*REG has the following format:

```
  N15 001uB4 0L ► uREG in BOOT mode
  N15 001u04x0L ► uREG in APPLICATION mode
   ------------
   |    |  ||||
   ------  |||MB software version [A..Z]
     |     |||    (presented in BOOT mode and APPLICATION mode)
     |     |||
prod. year ||reserve mark [generation]
number     ||
in year    |optional letter denoting application function,
           |                                  e.g. L (line)
           |                                       E (power station)
           |
           BOOT/Base version:
             Bn in BOOT mode, n=[0..9];
             xx in APPLICATION mode, xx=[00.99];
```

The serial number must correspond to the number on the rating label attached to the device enclosure.

17.3.3. PROJECT SIGNATURE

Project signature (ident 53) presents a 16-char signature of the active **APPLICATION** in *u*REG, according to following format:

```
DDDDDDDDCCCCCCCC
\------/\------/
    |       |
    |       code signature
    data signature
```

18. FAULT TROUBLESHOOTING

Unit faults can be generally divided into three classes:

1. abrupt faults caused by irreversible damage to one or more component(s), which prevents further operation of the device,
2. parametric faults caused by ageing or partial wear of components – gradual deterioration of device quality,
3. temporary faults caused by external or internal mechanical interruption, electromagnetic interference or due to errors in device software.

The following selection of recommendations for the measures in the event of fault (or suspected fault) concerns allowed actions to be taken by the operator.

→ Re 1:

- The controller is shut down (no signs of power supply) – Check the T0.5A fuse in the PS-0 module; if the fuse is burnt, a single attempt to replace it with an operational fuse is acceptable.
- The controller is supplied but the power LED is off – Record signs of the observed condition and make an attempt to reset the device by short (approx. 5 s) disconnection from auxiliary power supply.
- No recognition of the peripheral module based on the notification on the LCD screen – Once auxiliary supply is disconnected, make an attempt to replace the faulty module with an identical one.

If failed, please contact the manufacturer for assistance.

→ Re 2:

Most frequently, parametric faults of this class relate to two groups of circuits: measurement paths relating to analogue values (currents, voltages, temperatures, etc.) and sensitivity thresholds for digital inputs.

Current and voltage measurement paths are pre-adjusted for requirements ensuring indications within the proper accuracy class, at the final manufacturing stage of current and voltage transformer modules. For this purpose, instrument transformer boards are equipped with trimming potentiometers used to minimize measurement errors at selected characteristic curve points:

- for indications of CT-0 phase currents Ik = 2.0 A,
- for indications of earth-fault currents I0k = 0.5 A,
- for VT-0, VT-2, VT-3 phase currents Uk = 64.0 V,
- for the zero sequence voltage U0k = 20.0 V.

Consequences of imperfect pre-adjustment using potentiometers as well as ageing and ambient temperature effects can be additionally eliminated by the computer-based calibration mechanism dedicated to measurement paths. The mechanism is built in procedures of the system functor (called *KOREKTY / CORRECTIONS*). The functor provides a numerous group of corrective coefficients ('p'), which are time-varying (-128, +127), which determine resulting

values of attenuation/gain coefficients for most measurements taking place in the controller. For example, the value of the measured current 'Iw' is determined by the relationship:

Iw = Ip * (1 + p * 0.000122), where 'Ip' is the measurement value before calibration.

Thus, the measured value can be corrected within the range ± 1.55 %.
Derivative values (like power) can be corrected within a wider range ± 2.5 %.
The corrections are saved in the device as settings and can be changed during inspection of the device or its operation. However, it is necessary to follow standard values of respective current and voltages. Calibration can be performed for current-voltage characteristic points other than those used during factory calibration.

Unless in-house regulations state otherwise, it is recommended to conduct periodic checks of measurement paths associated with the unit every three years.

Observable ageing effects also refer to optoinsulation of digital inputs. This phenomenon is associated with penetration of contaminating particles into the semiconductor plate of the optical isolator light diode, causing gradual degradation. Intensity of this phenomenon depends on the ratio of lighting time to blanking and ambient temperature. Lasting for many years, deterioration of parameters can reach even 20 % of the initial performance. The ageing property was taken into account for parameters of digital input circuits. However, this fact must be mentioned and controlled. It is recommended to check switching thresholds of inputs after 10 years of operation.

→ Re 3:

Faults included in the 3rd class can result in two types of consequences:

- Momentary interruption of routine operation and immediate resumption. Then, the event is recorded in reports (it can be caused by internal interruption or a software error).
- Interrupted operation or computer crash without any attempt to reboot, which usually means an error in the device software. The controller will resume operation after restarting.

In each of the two cases, it is recommended to record data relating to event circumstances and the observable status of the device and contact the manufacturer's technical personnel.

19. PERFORMANCE AND INTERNAL TESTING

This section presents suggested instructions for laboratory and operational tests in the MV substation to determine *u*REG performance. These instructions are universal and relate to most hardware configurations and types of functional applications.

The instructions were developed based on observations and tests completed in previous years in relation to protection units, gained experience and general knowledge of electronics and electrical engineering.

The instructions are given in the form of a brief test report including:

1. different tests, with visual inspection and evaluation of the enclosure, the panel (LEDs, display, buttons, interfaces, termination strips for peripheral modules, IF-0 module lines, PS-0 power unit.

2. Power unit check:

The PS-0 power unit must be operated under the following conditions:

- set the power source to 95 V DC and apply auxiliary voltage, adjust LCD brightness to level 9,
- increase the supply voltage to 345 V DC,
- decrease the voltage to 88 V DC,
- set the source voltage to 230 V DC and measure the power input – power consumed from the source should not exceed 10 W.

3. Logic input check (under supervision of *Monitor3*); Digital inputs of peripheral modules should respond to the following activation/deactivation voltage thresholds:

- effective activation of inputs set to a high threshold 80 VDC
- effective discarding of inputs set to a high threshold 30 VDC
- effective activation of inputs set to a low threshold 21 VDC
- effective discarding of inputs set to a low threshold 10 VDC.

4. Relay check (under supervision of *Monitor3)*. Confirm relay switching on/off.

5. Check of errors of measurement paths relating to analogue values, including:

- phase currents If at desired points of the characteristic curve,
- phase voltages Uf at desired points on the characteristic curve (57.7 V AC and 100 V AC),
- frequency at the following points: 46.0 Hz, 50.0 Hz and 54.0 Hz during occurrence of phase voltages with a value of 30 V AC.

20. STORAGE / PRIOR TO OPERATION

*u*REG features a sophisticated design and requires fulfillment of specific conditions during storage.

The packaging guarantees protection from external factors which may result in damage. Therefore, DO NOT unpack the device during storage.

Packed *u*REG devices must be transported and handled with extreme caution to avoid shocks, maintaining the position indicated on the packaging.

Store the device in closed dry rooms (relative humidity 60 % to 70 %), free of corrosive gas vapors, at a temperature of +5 ^{0}C to +40 ^{0}C.
48 hours before the planned installation, unpack the device, remove the wrap and transfer the device to a room where the temperature is +18 ^{0}C to +30 ^{0}C, and relative humidity is up to 80 %. Leave the device aside and wait at least for 24 hours. After this time, the device is ready for operation.

In order to proceed with further *u*REG preparation for service, follow the description in earlier sections of this manual.

21. GUIDELINES FOR THE PURCHASER

The purchase order shall specify:

1. Type of functional **APPLICATION** and number, e.g.: wind plant 0E6, power plant 1E7, etc. (application type 0/1 specifies hardware configuration, the number 6/7 indicates the application version).

2. Mechanical design version:
   - 7-slot panel flush enclosure, integrated panel;
   - 7-slot panel surface enclosure, integrated panel;
   - separate panel flush installation w/ remote panel – 7, 10 or 14 slots

3. Type of operator panel:
   - GV vertical panel w/ color graphic display,
   - GH horizontal panel w/ color graphic display,
   - NV vertical panel with monochromatic alphanumeric display,
   - no panel to be supplied.

4. Type of 485 bus connections: wire (IF-0) / optical-fiber cable (IF-1/IF-2) / CAN-BUS (IF-4).

5. Number of power unit modules PS-0 / PS-1 (1 or 2)
   auxiliary voltage (standard PS-0 → 88 to 350 V DC, optionally PS-1 → 24 V DC).

6. Type of digital inputs: standard 220 V DC, optionally: 24 V DC, 230 VAC, 110 V DC.

Please submit your orders to:

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PL 60-649 Poznan

Tel./Fax: +48 61 8233748
E-mail: regulus@post.pl

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www.uREG.pl

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22. WARRANTY

A standard warranty period runs for 24 months after the date of sale.